



Implementation of Spiking Neural Network Izhikevich Model for Hand Written Character Recognition

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Abstract: Neural network concepts and principles appear to have great potential for solving problems arising in pattern recognition. Over the last decade, various spiking neural network models have been proposed, along with a similarly increasing interest in spiking models of computation in computational neuroscience. In this paper, for Pattern Recognition of Handwritten Characters, Spiking Neural Network's Izhikevich Neuron Model is used. Here for large scale simulations of the Izhikevich model we explore the expediency of using FPGAs. It has been observed that due to the accuracy, efficiency, power and simulation time; the Izhikevich spiking neuron model is best suited for large scale simulations.

Keywords: Pattern Recognition, Neural Network, Artificial Neural Network (ANN), Spiking Neural Network (SNN), Izhikevich Neural model, Field Programmable Gate Array (FPGA)

I. Introduction

Recognition is an important tool for decision making in human tasks. The term pattern recognition encompasses a wide range of information processing problems of great practical significance, from speech recognition and the classification of handwritten characters, to fault detection in machinery and medical diagnosis. Often these are problems which many humans solve in a seemingly effortless fashion. There are many pattern recognition tasks in speech and vision which we seem to perform effortlessly. Neural network concepts and principles appear to have great potential for solving problems arising in pattern recognition. Artificial Neural Network (ANN) is the second generation model and Spiking Neural Network is the third generation model of Neural Networks.

Spiking neural networks (SNN) fall into the third generation of neural network models, increasing the level of realism in a neural simulation [11]. SNNs incorporate the concept of time into their operating model which means that neurons in the SNN do not fire at each propagation cycle but rather fire only when a membrane potential – an intrinsic quality of the neuron related to its membrane electrical charge – reaches a specific value called as threshold. When a neuron fires, it generates a signal which travels to other neurons which in turn, increase or decrease their potentials in accordance with this signal [9].

In this proposed work, we are trying to show how Izhikevich neurons can be used for the pattern recognition. We have the Izhikevich model which is well known for producing all known firing rates pattern. It is combination of Hodgkin- Huxley model and computationally efficient Integrate and fire neuron model. Izhikevich model is designed and will recognize the input pattern of the image and generate the spikes. Here we adapt to the technique of using FPGAs for large scale simulations of the Izhikevich model. For this study we implemented a character recognition algorithm based on the Izhikevich model. Using the above model simulation results are obtained for recognition of handwritten characters and then measuring the Average firing rate, Accuracy, Efficiency and Simulation time.

II. Spiking Neural Network

SNNs overcome the computational power of neural networks made of threshold or sigmoidal units. Based on dynamic event-driven processing, they open up new horizons for developing models with an exponential capacity of memorizing and a strong ability to fast adaptation. Moreover, SNNs add a new dimension, the temporal axis, to the representation capacity and the processing abilities of neural networks.

The brain is a very complicated network of millions and millions of interconnected neurons that co-operate each other efficiently, process incoming signals and decide on actions. Typically, each neuron sends its signals out to over 10,000 other neurons. Biological neurons use short and sudden increases in voltage to send information, called action potentials or spikes or pulses. Neurological research has shown that neurons encode information in the timing of single spikes, and not only just in their average firing frequency. This allows incorporating spatial-temporal information in communication and computation, like real neurons do. So instead of using rate coding, these neurons use pulse coding mechanisms where neurons receive and do send out individual pulses, allowing multiplexing of information.

Recently several SNN models have been proposed. Several studies compare 11 spiking neuron models base on their biological plausibility and computational complexity. Of these models, current studies of SNN models are generally using the Hodgkin-Huxley, leaky integrate-and-fire and Izhikevich model. The integrate-and-fire model is the most commonly utilized – both for algorithmic studies and hardware implementations. However the integrate-and-fire spiking neuron model is not very biologically accurate and is unable to reproduce the spiking behavior of many neurons. Izhikevich model is almost as accurate as the highly detailed Hodgkin-Huxley neuron model but with the low computational cost of the integrate-and-fire model.

III. Izhikevich Neuron Model

Izhikevich [6] proposed a new spiking neuron model in 2003 which is based on only two differential equations.

$$v' = 0.04v^2 + 5v + 140 - u + I \quad (1)$$

$$u' = a(bv - u) \quad (2)$$

$$\text{if } v \geq 30mV \quad (3)$$

then $v \leftarrow c$,

$u \leftarrow u + d$

where the state variable v is the neuron membrane potential, while the state variable u is the neuron recovery variable and I is the neuron current.

The condition $v = 30mV$ is the spiking condition. Whenever this condition is met, the neuron “fires” and then goes back to the reset state expressed in the same formula.

The constants 0.04, 5 and 140 have been chosen by Izhikevich; using these it is possible to simulate at least 20 biologically meaningful spiking behaviors. a , b , c and d are the four dimensionless parameters of the Izhikevich neuron model.

- The parameter a describes the time-scale of the recovery variable u . Smaller values result in slower recovery;
- The parameter b describes the sensitivity of the recovery variable u to the sub-threshold fluctuations of the membrane potential v . Greater values couple v and u more strongly resulting in possible sub-threshold oscillations and low-threshold spiking dynamics;
- The parameter c describes the after-spike reset value of the membrane potential v caused by the fast high-threshold K^+ conductance;
- The parameter d describes after-spike reset of the recovery variable u caused by slow high-threshold Na^+ and K^+ conductance.

It takes only 13 floating point operations to simulate 1 ms of the model, so it is quite efficient in large-scale simulations of cortical networks.

In our system, we applied the Izhikevich model as a compromise for the biophysical similarity and computational power. The model is close to the Hodgkin-Huxley model in biological plausibility, but it is similar to the leaky I&F model in computational complexity.

IV. Hardware Implementation

To explore the feasibility of the proposed architecture and spiking neuron model explained in the previous section, we implemented the SNN structure on an Altera Cyclone II 2C35 FPGA. Figure 1 shows the overall design of this system.

The aim here is to observe the neuron-firing activity and recognize the alphabets on an oscilloscope where the neuron model is being modeled using Hardware Description Language.

To observe the required spikes given by the variable v (membrane potential), the audio CODEC available with the DE2 board is included. And to control the CODEC and its interface (in this case it is I2C) controllers are modeled using HDL.

A. Simulation Parameters:

The setup for this project involves:

1. Altera DE2 Board, Cyclone II FPGA, EP2C35F672C6.
2. A Digital Storage Oscilloscope (Tektronix).

Some information about the two devices:

AUDIO CODEC

The WM8731 is a low power stereo CODEC with an integrated headphone driver. The 24-bit Audio CODEC on DE2 is implemented by the WM8731. This chip provides Microphone in, Line In, and Line Out connectors. By using the I2C bus on DE2 board, the sample rate can be adjusted from 8 KHz to 96 KHz. This device is controlled via a 2 or 3 wire serial interfaces. The interface provides access to all features including volume controls, mutes, de-emphasis and extensive power management facilities.

I2C BUS

The interface available with DE2 board is I2C. I2C is a serial protocol for two-wire interface to connect low-speed devices like microcontrollers, EEPROMs, A/D and D/A converters, I/O interfaces and other similar

peripherals in embedded systems. I2C bus is popular because it is simple to use. There can be more than one master, only upper bus speed is defined and only two wires with pull-up resistors are needed to connect almost unlimited number of I2C devices. I2C uses only two wires: SCL (serial clock) and SDA (serial data). Both need to be pulled up with a resistor to $+V_{dd}$. Each slave device has a unique address. Transfer from and to master device is serial and it is split into 8-bit packets.

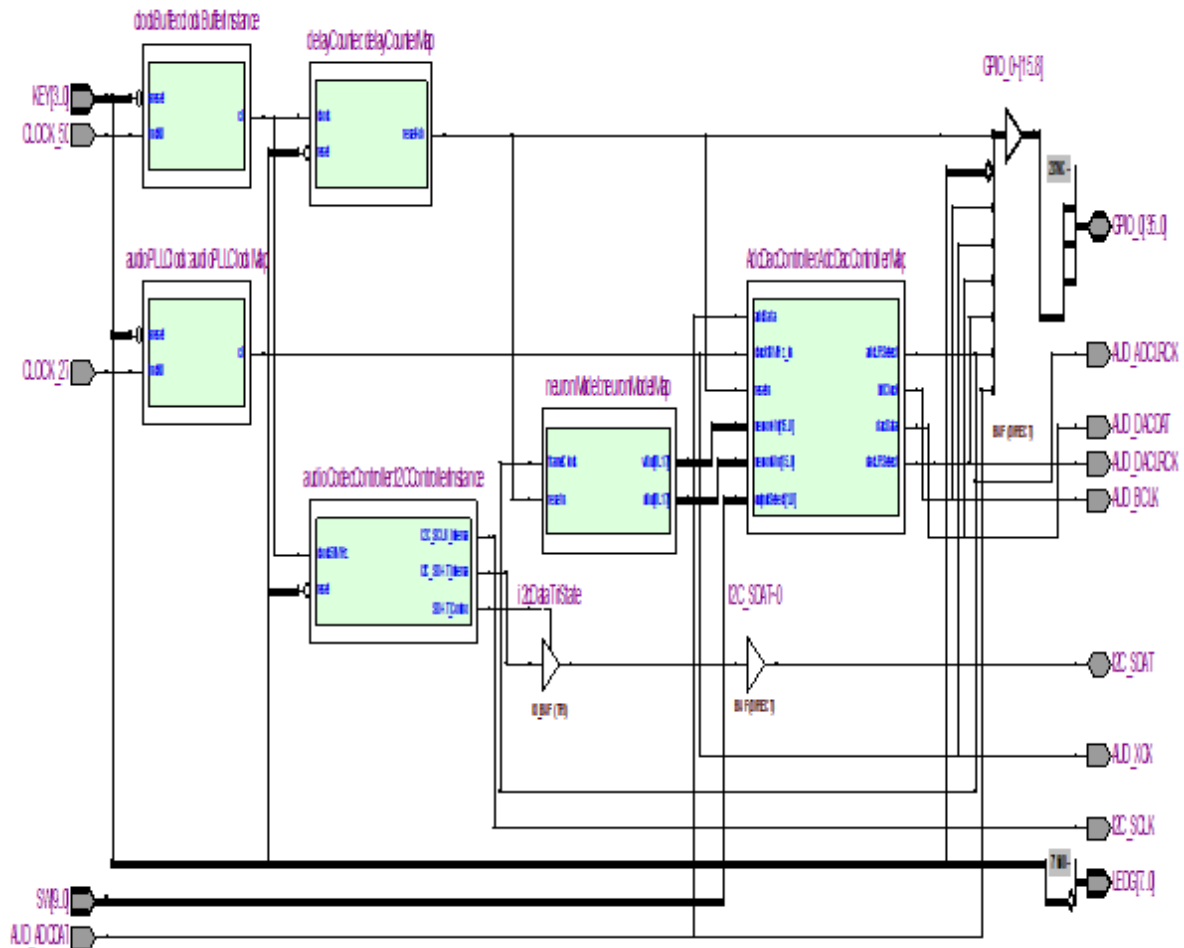


Figure 1 RTL view of the complete design

The digital form of the membrane potential v is to be converted into analog (spike) and for that reason the output (LINE OUT) of the audio CODEC is connected to the channels of the DSO. A probe having double headed BNC connectors at one end and a 3.5 mm Jack (for LINE OUT) at the other end is used for observing the required neuron spikes. The DSO has an inbuilt option of saving the waveform as an image. The results are obtained in image form (JPEG) from the DSO.

V. Results

In our proposed work, by using the Izhikevich Spiking Neural Network model we implemented a character recognition algorithm. Using FPGA the simulation results for the English characters 'W', 'x', and simulation result for digit '1' are obtained and observed at the output of DSO. The spikes produced with the Izhikevich neuron model on FPGA for English characters are as follows:



Figure 2 Input image for character 'W'



Figure 3 Recognition of character 'W' by Izhikevich Neuron Model



Figure 4 Input image for character 'x'

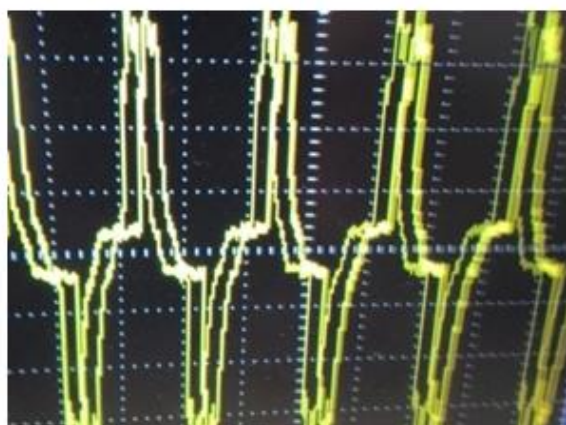


Figure 5 Recognition of character 'x' by Izhikevich Neuron Model



Figure 6 Input image for digit '1'

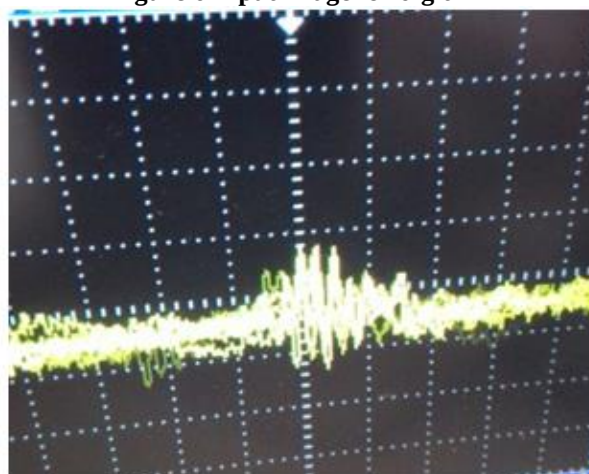


Figure 7 Recognition of digit '1' by Izhikevich Neuron Model

Parameter	
Area	1325 Logic Elements
Timing	57.79 MHz
Accuracy	20/25 = 80%

Table 1 Resource Utilization Summary

Table 1 shows the resource utilization summary of the FPGA based implementations and their timing breakdowns. The “Area” is the number of logic elements utilized in the FPGA. The “Timing” is the time required to read the simulation cycle count needed for recognition. The “Accuracy” is the total number of characters recognized accurately i.e. every 25 sample characters, 20 characters showed accurate results.

VI. Conclusion

In image pattern recognition, a large number of complex computations are involved. This in turn reduces the speed of pattern recognition. In conventional techniques it has been found that not only speed is slow but accuracy of the results is also compromised. In our project we tried to focus on this aspect. To solve this problem we proposed a new image pattern recognition method in which spikes are used to recognize the pattern based on spiking neural network. We implemented an Izhikevich neuron model using FPGA to get more accurate error free result. In our proposed work, out of 25 sample characters, 20 characters showed accurate results, thus making the Izhikevich model significantly more attractive for large scale error free simulations. This research work mainly focus on recognition of one input image at a time. But in future we can include the recognition of text, recognition of objects.

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