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Literature Review on Flip-Flops for a novel design at Low Power and High Speed

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Abstract: Flip-flop (FF) being a storage element occupies a significant space in digital circuit design such as register, counter and finite state machine. In view of its huge applications, it is important to understand its operation in details obtaining a high level of insight into its various performance metrics such as speed, power dissipation, hold-time, set-up time and area. Thus, there is a significant research effort on FF which revealed various techniques for its performance improvement and optimization

Keywords: Counter, Hold time, Finite State Machine, Registers Storage Element.

I. Introduction

There can be various type of FF, each having advantage/disadvantage over one another. D-FF is among commonly used FFs because of its relatively simple operation. It can be either of static or dynamic type as shown in Fig.1.1.(A) and Fig.1.1.(B) In static flip-flop output data is stored using latch whereas in dynamic flip-flop output is stored by using the node capacitance and thus it needs clock pulse at regular interval to preserve data at appropriate logic level. Static type flip-flop usually utilizes more transistor than dynamic type. Glitches and charge sharing are two drawbacks that happens in dynamic type D-FF, resulting in a different state of the circuit node voltage.

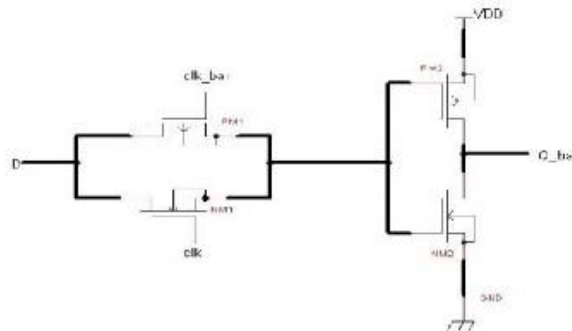


Fig 1.1.(A) Dynamic D-FF

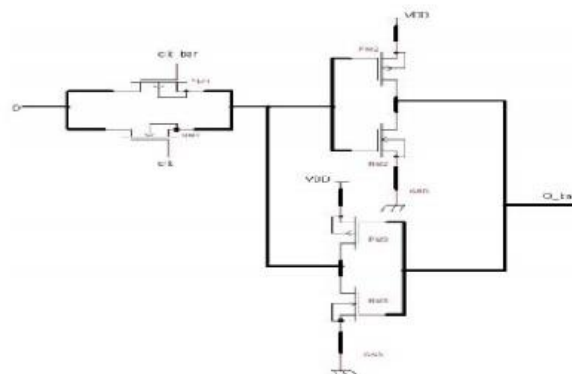


Fig 1.1.(B) Static D-FF

The FF can be either level or edge triggered, and thus can be classified as follows:

1. Positive level triggered flip-flops

2. Negative level triggered flip-flops
3. Positive edge triggered flip-flops
4. Negative edge triggered flip-flops
5. Dual edge triggered flip-flop

II. Positive Level Triggered Flip-Flops

These flip-flops operate when clock is at logic high level, and don't respond to any transition in clock or when clock is at low logic. Fig.1.2 (A) and (B) shown typical example of +ve level triggered static and dynamic type D flip-flop respectively. It is clear that input data is transfer to output when clock is at logic high level.

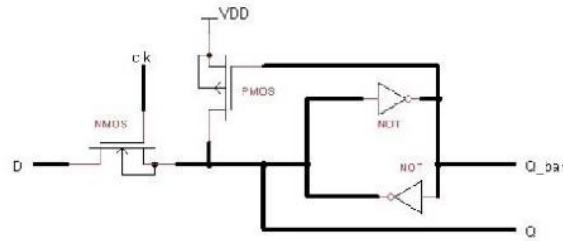


Fig 1.2.(A) +ve level static D-FF

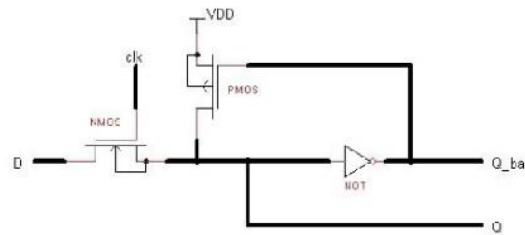


Fig 1.2.(B) +ve level dynamic D-FF

III. Negative Level Triggered Flip-Flops

As name specifies, -ve level triggered flip-flops work only at low logic of clock pulse. Circuit schematic of -ve level triggered flip-flops using transmission gate shown in Fig.1.3. (A) and (B). Transmission gate based flip-flops do not need voltage boost circuit mechanism as in Fig.1.2 (A) and (B) which are based on pass transistor.

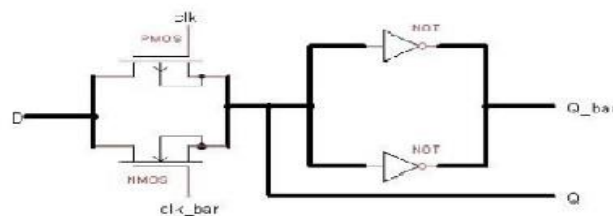


Fig 1.3.(A) -ve level triggered static D-FF

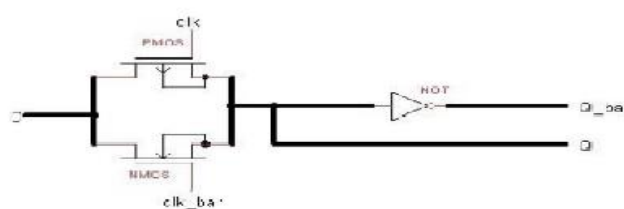


Fig 1.3.(B) -ve level triggered dynamic D-FF

IV. Positive Edge Triggered Flip-Flops

When rising edge of clock is utilized to trigger the flip-flop, such flip-flops comes under category of +ve edge triggered flip-flops. Schematic of +ve edge triggered flip-flop shown in Fig.1.4.(A) and (B).

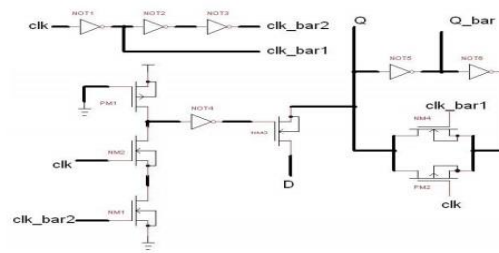


Fig 1.4.(A) +ve edge triggered static D-FF

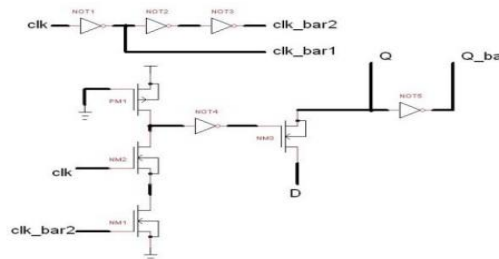


Fig 1.4.(B) +ve edge triggered dynamic D-FF

V. Negative Edge Triggered Flip-Flops

In contrast to +ve edge triggered flip-flop, -ve edge triggered flip-flop works on falling edge of clock.

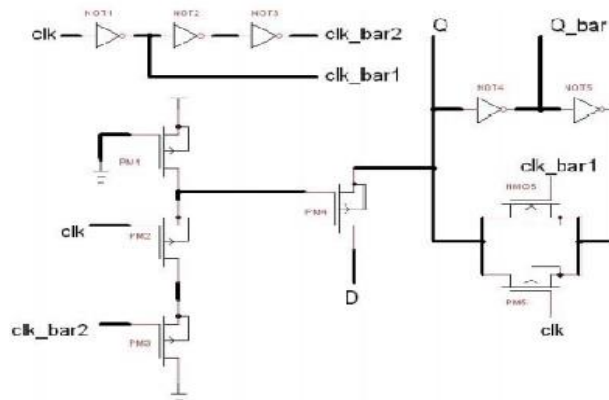


Fig 1.5.(A) -ve edge triggered static D-FF

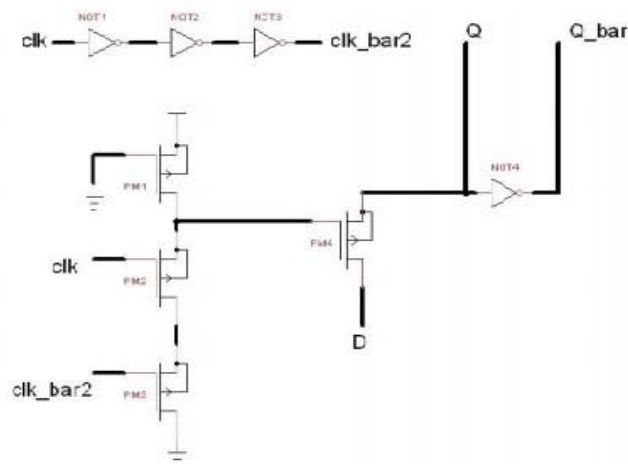


Fig: 1.5.(B) -ve edge triggered static D-FF

VI. Dual Edge Triggered Flip-Flops

In dual edge triggered flip-flops, both edge of clock is utilizes to sample the input data. Simple Dual edge triggered flip-flop can be made by parallel combination of +ve edge and -ve edge triggered flip-flop as shown in Fig.1.6.(A).

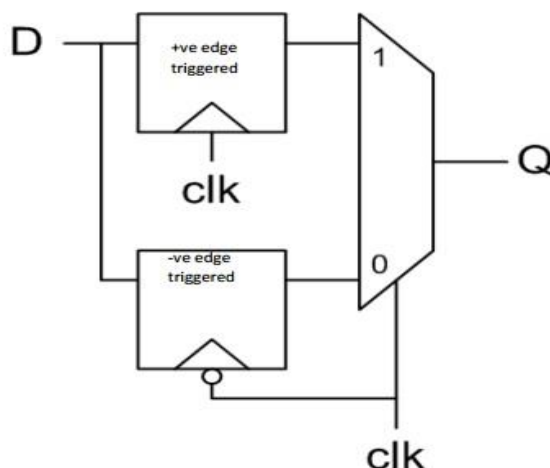


Fig 1.6.(A) Simple configuration for Dual edge triggered D-FF

But structure shown as above is bulky and consumed more power another kind of structure for dual edge triggered D-FF shown in Fig.1.6.(B) this is much efficient design but having less speed than FF shown in Fig.1.6.(A).

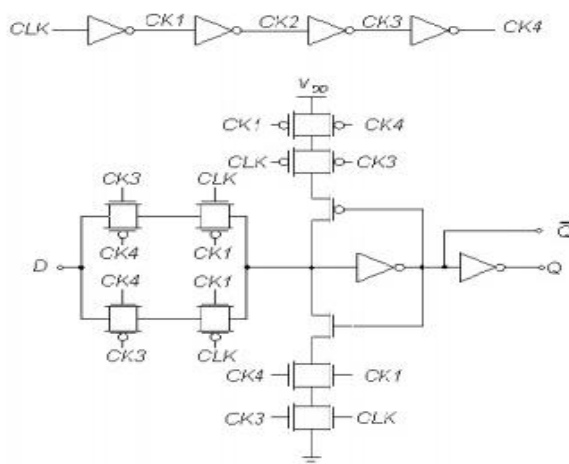


Fig 1.6.(B) Another configuration for dual edge triggered flip-flop

Following Fig.1.6.(C) shows the output for +ve edge triggered flip-flop and dual edge triggered flip-flop for same data sequence and clock pulse.

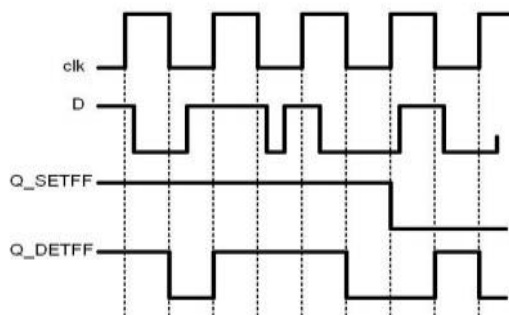


Fig 1.6.(C) output data for single edge triggered flip-flop (SETFF) and dual edge triggered flip-flop (DETFF)

The problem with level triggered flip-flop is that inputs change the outputs many times for single clock pulse

and condition can be even worse when output is feedback to the input. Race-around condition is the key disadvantage of level triggered flip-flops. When Level triggered FF work in toggle mode then output changes many times for single clock pulse that is undesirable, this phenomenon known as race-around condition.

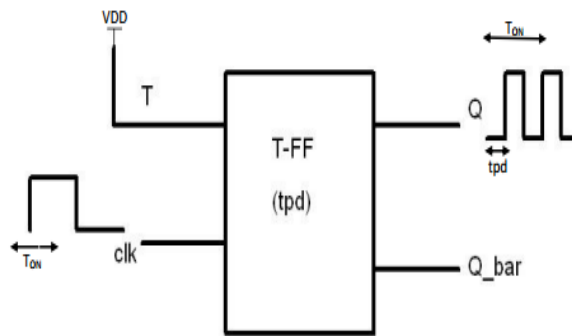


Fig 1.6.(D) race around condition in T-FF

- To avoid race-around condition master-slave flip-flop or following clock scheme can be used:
- I. ON time of clock pulse (T_{ON}) < Propagation delay (t_{pd}) of +ve level triggered flip-flop but overall $T_{clk} > t_{pd}$
 - II. OFF time of clock pulse (T_{OFF}) < Propagation delay (t_{pd}) of -ve level triggered flip-flop but overall $T_{clk} > t_{pd}$

Besides arrangement in clock duty cycle, master-slave or edge triggered flip-flops are widely used to avoid race-around condition. In master-slave flip-flop [2], output is taken from slave whereas input signal is fed to its master as shown in Fig.1.6.(E).

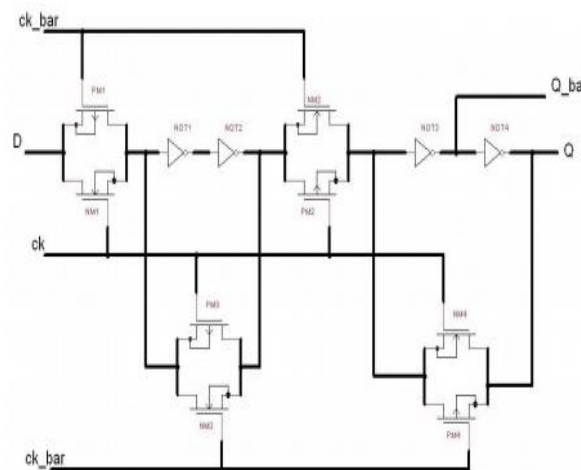


Fig 1.6.(E) Master-slave D-FF

Master and slave is on opposite phase of clock therefore master and slave run alternatively. Master-slave flip-flops require more number of transistor thereby consumed more area and power whereas edge triggered flip-flops are small, fast and consumed less power.

VII. Summary

Single edge triggered flip-flops [7], (i.e. positive (+ve)/negative (-ve) edge triggered flipflops) respond only at level transition of clock it means +ve edge triggered flip-flops work when clock transit from low to high level and -ve edge triggered flip-flops work when clock transit from high to low level. It is noteworthy that in single edge triggered flip-flops (SETFFs), one edge of clock is not utilized for data modification. However, voltage at the internal nodes of circuit changes on the clock edge and thereby resulting in significant switching power consumption during the unutilized clock edge. On the other hand, dual edge triggered flip-flop (DETFF) operates with both edge of clock. To achieve same data throughput DETFF requires half of clock pulse and power consumption is significantly lower in DETFF. For example to send data sequence 1101 SETFF require four clock pulse while DETFF requires only two clock pulse normal/perpendicular to the surface.

VIII. Conclusion

In order to integrate more number of functionalities in an Integrated Circuits (ICs) with given area, the devices are reducing in size in an aggressive manner. Such an increase in number of switching nodes, and a miniaturization of device size, both dynamic and static power dissipation are increasing at an alarming rate with the technology generation. This is not only a serious problem for portable application but also for high performance desktop application since it requires a costly cooling mechanism. As In small chip area billion of transistors can be mend but it cost increment in power dissipation through device. Depending upon application for which a device is used power dissipation also differ. Reliability of chip degraded with higher power dissipation. It is tough job to optimize the device for all application in concern of power dissipation. An ideal device has to be fast and must work at low power, but in practical sense delay and power dissipation cannot be reduce simultaneously. There is a compromisation between delay and power for a device. In general both delay and power are inversely proportional to each other for a device, thereby for a device power delay product (PDP) must be as small as possible. To stand in current semiconductor market, a chip must have low PDP. Most of electronic circuit based on MOS device, lots of research have been done to reduce power and delay [8, 9, 10]. Flipflops are basic components for sequential circuits. Normally 20 to 45 % of total power is dissipated by flip-flops. So FFs needs high attention in design of low PDP system.

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