

Design and Implementation of Two Stage High Gain Op-Amp with Current Buffer

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Abstract: This paper presents a fully differential compensation with current buffer two stage op-amp using a CMOS technology. In this circuit we achieve a high B.W is suitable for a high speed application. The proposed amplifier has been used 0.18μm technology. The output swings, CMRR, are show in this circuit. In proposed amplifier we achieved UGB and phase margin (5.82, 63.97). Fully differential stage technology used operational amplifier along with the optimization of B.W, CMRR and Gain at 1.8v. This technique is stable the output result and optimize the amplifier performance.

Index Terms: Two stage CMOS amplifier, High B. W design, Analysis, low distortion.

I. INTRODUCTION

Analog ICs is becoming most popular by reducing its transistor channel length and supply voltages. For better performance and stability we have to reduce the structure size. Negative feedback connection and frequency compensation is necessary for closed loop stability. MOS amplifier design deals with the balancing of performance through the variation of several device level parameters for e.g. FET channel width length, and inversion levels. These parameters strongly influence the speed, gain, noise, immunity and power dissipation of given circuit design [1]. The digital system designing is continuously pushing for increasing speed of minimum size devices. To achieve higher voltage gain and less complicated operations, longer channel are now being employed avoiding the short channel effect. But in the designing of higher bandwidth amplifiers, there is a need to understand short channel effect on overall circuit behaviours [1].

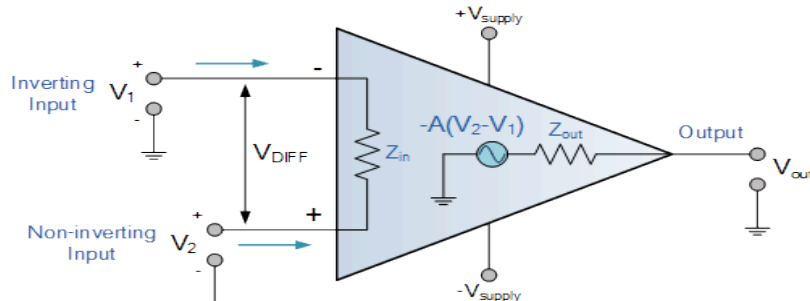


Fig. 1. Structure of operational amplifier

II. Differential Amplifier

A difference between the amplification of two different voltage input with no feedback is differential amplifier. In practical use its too high and cannot controlled its gain in difference amplifier we have only used one inputs that is connected to the amplifier using input terminals 'inverting and non inverting'. Only one input is being amplifier and another one is connected to the ground, but today we can easily amplify both the inputs voltage signals is connected together at a same time to produce another common type of amplifier.

Differential amplifier equation:

$$V_{OUT} = R_3/R_1 (V_2 - V_1)$$

If all the resistors are same value

$R_1 = R_2 = R_3 = R_4$ that means the circuit is unity gain and the gain of voltage = one or unity.

For a better performance and improved the gain B. Wand PSRR results we have to provide a compensation. Compensation blocks a common gate MOS overcomes the limitation of the current buffer, which decreases the out swing result. The much value of C_c reduces the noise performance and power consumption. [2]

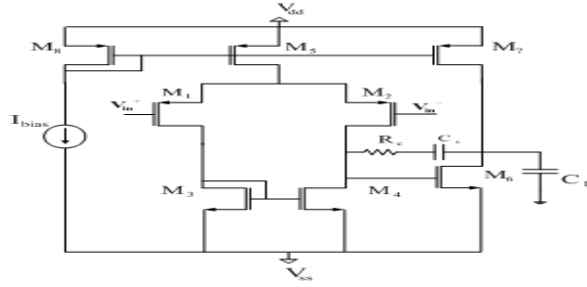


Fig. 2. Two Stage Operational Amplifier

In strong inversion region the equations of the MOSFET are:

$$I_D = U_{n,p} C_{OX} \frac{W}{L} V_{eff}^2 \quad (1)$$

$$G_m = \sqrt{2} U_{n,p} C_{OX} \frac{W}{L} I_D \quad (2)$$

$$G_m = \frac{2 I_D}{V_{eff}} \quad (3)$$

V_{eff} = effective voltage (NMOS/ PMOS)

III. DESIGN PROCEDURE OF OP-AMP

Step 1: Consideration For Gain And Bandwidth

Small signal transfer function is given in equation (4):

$$A(s) = \frac{W_{gbw}}{s} \times 1 + \frac{C_c + C_{gs6}}{G_{m6}} / s^2 (C_L C_{gs6} / C_c G_{m6} \times C_c + C_{gs9} / G_{m9}) + s (C_L C_{gs6} / C_c G_{m6} + C_{gs6} / G_{m6}) \quad (4)$$

DC gain and UGBW can be given as:

$$W_{GBW} = A_{dc} W_{p1} = g_{m1} / C_c \quad (5)$$

Step II: Output Swing

As the analog ground we assume that $(V_{DD}/2)$, respectively are

$$V_{OS}^+ = V_{DD}/2 - V_{eff6} \quad (7)$$

$$V_{OS}^- = V_{DD}/2 - V_{eff7} \quad (8)$$

Step III: Input Common Mode Range (+ve and -ve CMR)

In figure 2 it is easy to show that

$$V_{CMR}^+ = V_{DD}/2 - V_{eff3,4} + V_{tn} \quad (9)$$

$$V_{CMR}^- = V_{DD}/2 - V_{eff1,2} - V_{tn} - V_{eff5} \quad (10)$$

Step IV: Slew Rate

The external and internal slew rate can be found to be

$$SR = I_{D5} / C_c \quad (11)$$

$$SR = I_{D7} - I_{D5} / C_L \quad (12)$$

From (11) and (12), we obtain

$$I_{D7} = SR (C_c + C_L) \quad (13)$$

From (3), (5), (11)

$$V_{eff(1,2)} = SR / W_U \quad (14)$$

Where V_{eff} = Input voltage range

For increasing this range V_{eff} we easily improved slew rate and constant bandwidth

Step V: Offset Minimization

If the impedance matching is perfect and input first stage is connected to the ground then, $V_{SD3} = V_{SG3} = V_{SD4} = V_{SG6}$. These types of condition reduce the output stage current to improve the input impedance.

III. Amplifier characteristics

Amplifier characteristics like voltage gain, non linear distortion and bandwidth act as a function of channel length and inversion

- VOLTAGE GAIN:** Often a voltage gain of CMOS amplifier with current source load is assumed to be proportional to channel length. But this assumption fails to consider the inversion level. In fact the short channel devices are often continue to effectively amplify signal at inversion level

- **TOTAL HARMONIC DISTORTION:** For a given input harmonic distortion always decreased with channel length across all the three region of inversion with addition reduction in weak inversion region. The additional reduction is due to constant voltage gain in weak inversion region
- **GAIN- BANDWIDTH:** In circuit that required high bandwidth, the gain bandwidth is an important factor of consideration. The voltage GBW is defined as the product of the magnitude of mid-band voltage gain and 3-db bandwidth of an amplifier stage.

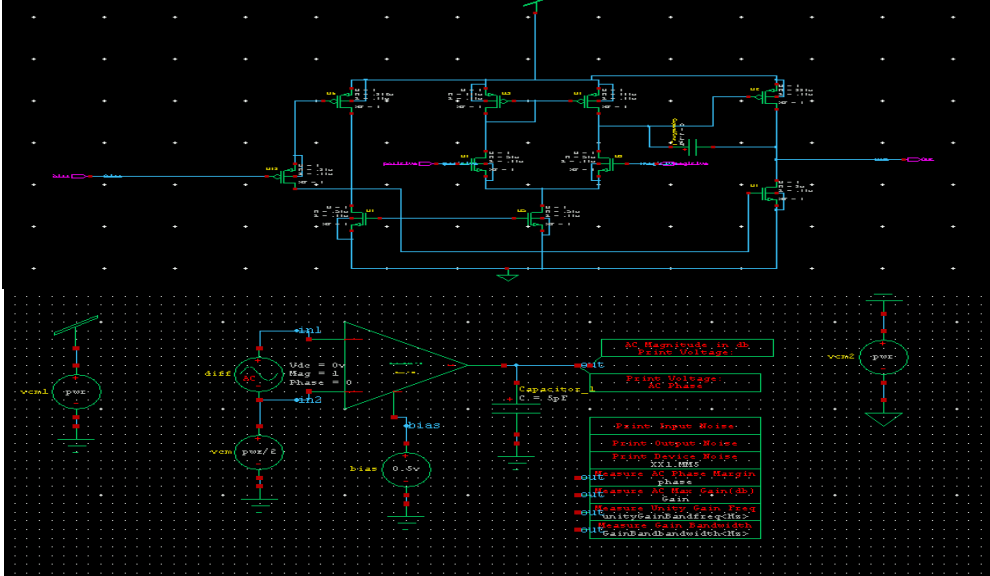


Fig. 3. Two-stage Differential Amplifier

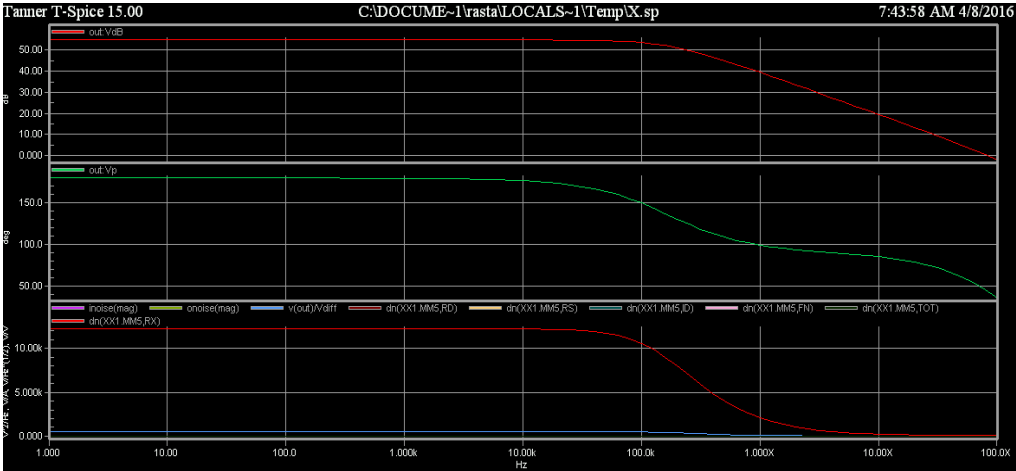


Fig. 4. Simulation result

IV. DESIGN OF TWO STAGE DIFFERENTIAL OPERATIONAL AMPLIFIER

The two stage operational amplifier is designed in 0.18um CMOS technology. The procedure variables are specified in table 1 and other designed specification in table 2 that are used for target specifications.

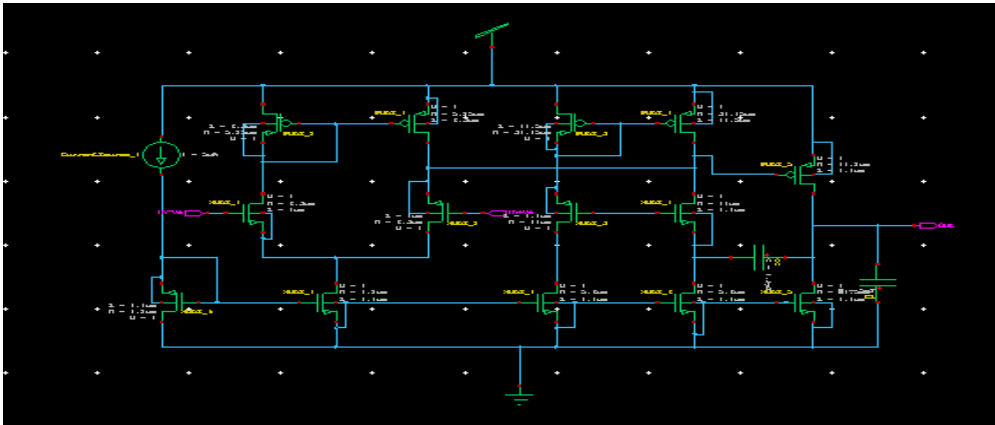
DESIGN PARAMETERS:

TABLE 1.

DEVICES	WIDTH AND LENGTH
N1, N2	6.3/7
N3, N9	4.2/1.4
P1, P2	5.25/6.3
N4,N5	14/1.4
N8, P5	5.6/1.4, 31.15/17.5
P3, P4, Cc	31.15/1.4, 0.5pF
C _L	5pF

TABLE 2.

PROCESS PARAMETER	NMOS	PMOS
$\mu(\text{Cm}^2/\text{VSec})$	421.38	155.52
V(Volt)	0.549	-0.680



V. SIMULATION RESULT

In figure 5 and 6 a frequency versus Gain response and slew rate are shown. The simulation result and main goal are given in table 3. Comparison of result with the result [2].

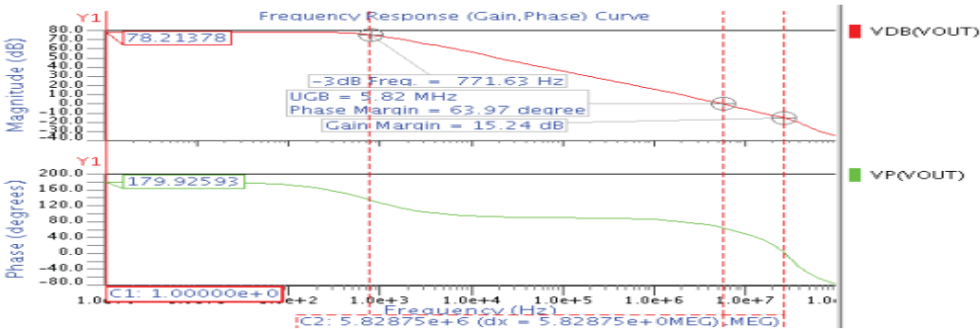


Fig. 5. Frequency response

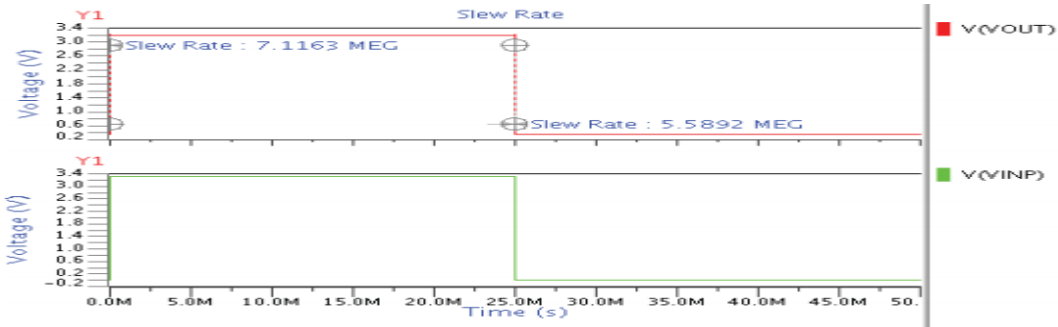


Fig. 6 . Slew Rate

TABLE. 3 Simulation Result

Specifications parameters	target	[2]	results
Low frequency gain(db)	>80	81	79.21
UGB(MHz)	5	5	5.82
Phase margin(degree)	65	65	63.97
Slew rate(+ve)	5.5	6.5	7.11
Slew rate(-ve)	5.5	5.9	5.57
CMRR	-		89.05
Power dissipation	-	378	143.34

VI. CONCLUSION

The characterization and optimization of MOS amplifier of consideration of voltage gain, THD and GBW and their relation to device channel length and channel inversion in common source stage further it is formulated that if the gain requirement is coupled with use of long channel devices then it is advisable to move a short channel device in order to increase circuit speed and lower distortion. The proposed designed is carried out with 0.18 μm technology with supply voltage 1.8V. The results show the improvement in UGB, slew rate

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