

Performance Evaluation of FinFET Based 8T SRAM Cell

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Abstract- In the design of memory, the estimation of dynamic power, dynamic current, leakage current and power of leakage are very essential, especially for low power applications. In this paper, we propose a FinFET base 8T Static Random Access Memory (SRAM) cell. FinFETs also promise to improve the difficult performance report power of compromise. FinFET can be used to reduce the leakage current and power of leakage. The purpose of this paper is to reduce the leakage current, power and improve the dynamic current, power of FinFET based 8T SRAM cell. The present paper represents the simulation of 8T and the analysis of SRAM different parameters such as dynamic current, dynamic power, leakage current and power of leakage. All the simulation results are carried out in cadence virtuoso simulator.

Keywords- Static Random Access Memory (SRAM); FinFET; Read Word Line (RDWL); Read Bit Line (RDBL); Write Word Line (WWL); Drain Induced Barrier Lowering (DIBL)

I. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) Technology is facing enormous challenges to channel length below 90nm, such as Gate leakage current, under the threshold leakage current and drain induced lowering of the barrier (DIBL) current, any FinFETs overcome these problems in the CMOS. It is clear that the future of the technology of materials should show greater mobility, greater stability, and the scalability against the process and reduces the effects of variations of short channel effects. Due to the scaling of deep submicron processes in the memory, the variations in temperature, power supply voltage and the variations of the process put the most important challenges for the future of the design of the memory and the high-performance device [1-3]. At this time, it has been proposed to replace the CMOS transistors in the SRAM with FinFET [4-5]. These FinFETs have a weaker effect of short-channel, leakage current and power leakage by report to the CMOS transistor. While the search for solutions with a leakage current, higher integration, and the stability of performance of lower power, FinFETs has given the next generation of 8T SRAM cell [6-7]. As the technology scales down, the supply voltage must be decreased such that dynamic power can be maintained at reasonable levels. However, due to the scalability, energy consumption can be increased due to a leakage of current has also increased and it is used for low power applications. This paper presents information on how to check the leakage current, leakage of power supply and how to optimize the dynamic power in the SRAM cell [8]. An overview of this document is organized as follows. Section 2 illustrates the structure of the FinFET device. Section 3 describes the FinFET based 8T SRAM cell. Section 4 gives the results of the simulation. The final section presents the conclusions of this work.

II. FINFET DEVICE STRUCTURE

In accordance with the propose of a method is provided to build a fin type field-effect transistor (FinFET) which is well suited to the manufacturing processes of MOSFET in bulk. The FinFET device includes a thin channel fin position of silicon on an insulating layer with the gate overlapped the sides of the fin. Therefore, the layers of inversion are created on the sides of the channel such that the two gates control the whole of the channel film and limit the modulation of conductivity of channel by the source and the drain.

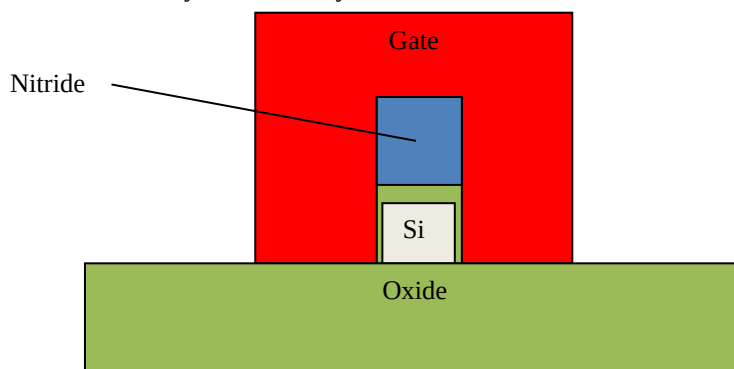


Fig. 1 Double Gate FinFET

In most cases, the length of the channel is greater than the width of the film to channel such that the channel of the FinFET is like a long thin film. The FinFET channel fin effectively reduces the SCE and strengthened the drive current.

Fig.1 shows the fundamental structure of a FinFET, the device is created on a thin layer of silicon. The nitride was deposited on the top of the fin of silicon on a thin pad thick oxide to keep the fin of silicon for the duration of the gate poly-SiGe engraving. The gates are formed to the vertical sides of the fin with a thin oxide layer. In the FinFET, the W_{fin} width of fin is much larger than its height T_{fin} and oxides of gate to side walls are much thicker than the oxide of gates at the top, the device is called as a structure with single gate. Fig.1 shows that the component vector of the density of electron current is perpendicular to the FinFET.

III. FINFET BASED 8T SRAM CELL

The FinFET based 8T SRAM cell consists of two cross coupled inverters and two n-channel FinFET based access transistors shown in Fig.2; these cross coupled inverters are called as a latch. The latch has four transistors; each bit in a FinFET based SRAM is stored on four transistors. The drain terminal of n-channel FinFET based access transistors are connected to the latch inputs and source terminals are connected to the bit line and bit line bar. The additional n-channel FinFET based transistor M7 is connected to the storage node Q and M8 transistor are connected to the Read word and read bit lines (RDWL and RDBL).

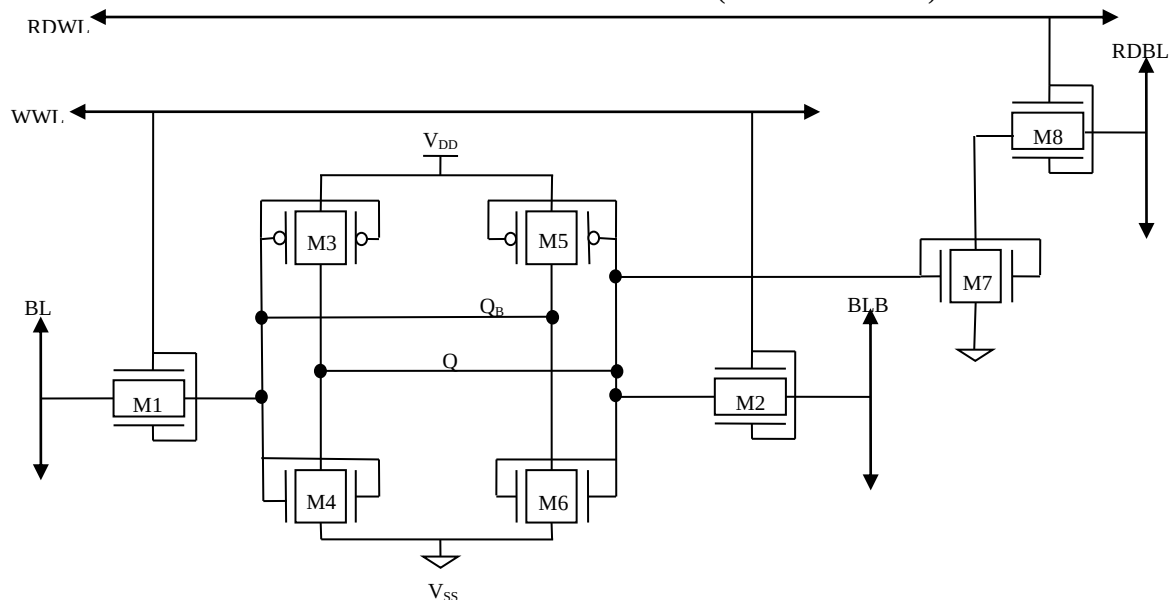


Fig. 2 FinFET based 8T SRAM Cell

FinFET based SRAM stability is characterized by the data retention stability through a read operation. In 6T SRAM cell design with FinFET, the data storage nodes are accessed directly through the n-channel FinFET based access transistors connected to the bit line and bit line bar. The storage nodes are cut off due to the voltage division between the latch and the n-channel FinFET based access transistors during a read operation.

Separation of data retention component and data output component means there will be no relationship between I_{cell} and read SNM. To overcome the problem of destruction of data in FinFET based 6T and 7T SRAM cells during the read operation [9-10], we implement the FinFET based 8T cell, for which separate word lines and read/write bits are used to separate the output data and the data retention element. In turn, the implementation provides a cell read disturb free operation. As shown in fig.2, FinFET based 8T SRAM cell has 30% more area than a conventional FinFET Based 6T SRAM cell. The 30% area overhead is composed of not only the two added n-channel FinFET transistors but also of the contact area of the word-line for write (WWL) operations. While WL contact area is conventionally assigned to the boundary line between two FinFET Based SRAM cells, in this FinFET based 8T SRAM cell the WWL contact area is assigned to within a cell.

IV. SIMULATION RESULTS

The proposed 8T SRAM cell with FinFET has been designed using Cadence; all the waveforms have been generated on SPECTRE simulator. Clearly we see that the proposed FinFET based 8T SRAM cells show good performance in terms of dynamic current, dynamic power and improve the leakage current, leakage power as compared to the FinFET based 6T and 7T SRAM cells.

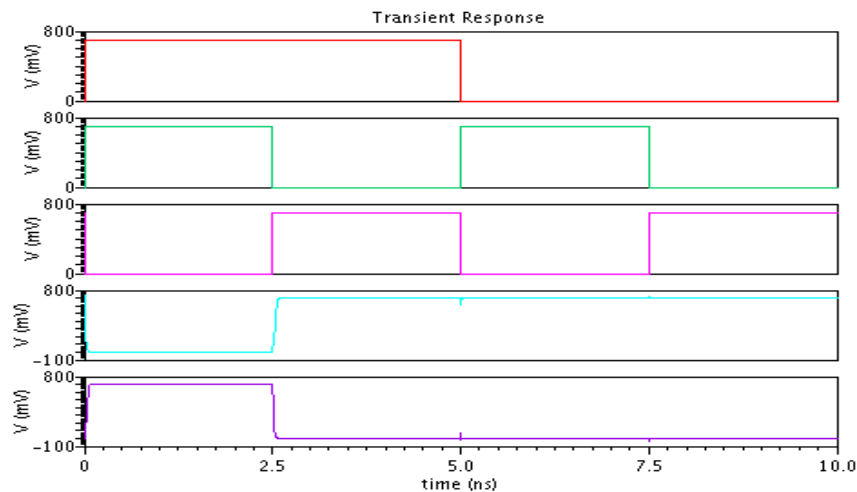


Fig. 3 the waveform for write operation in FinFET based 8T SRAM cell

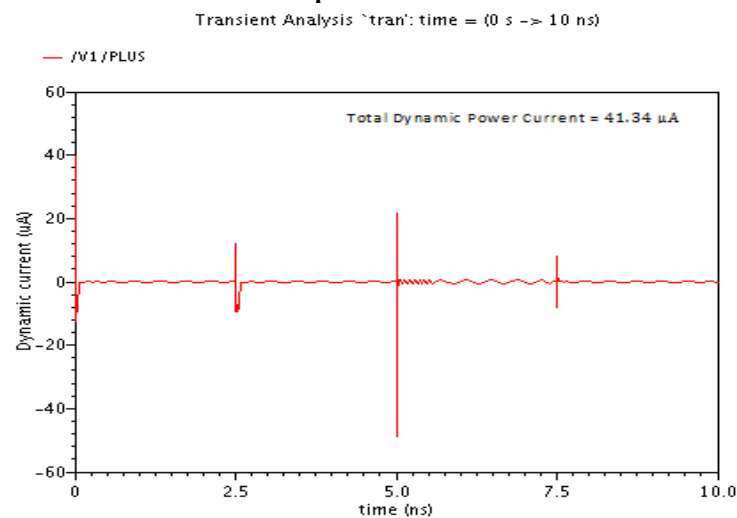


Fig. 4 shows the waveform for total dynamic current in FinFET based 8T SRAM cell

Figure 3 shows the waveform for write operation in FinFET based 8T SRAM cell. In the waveform BL and BLB refers to bit and bit line bar respectively. The voltage level on every source has been kept at 0.7V. In Figure 3, when write word line (WWL) is high the output states of Q and QB change according to the BL and BLB and when WWL goes low the SRAM retains the data.

Figure 4 and 5 shows the waveform for total dynamic current and total dynamic power in FinFET based 8T SRAM cell. The total dynamic current and total dynamic power are $41.34 \times 10^{-6} A$ and $28.94 \times 10^{-6} W$ respectively.

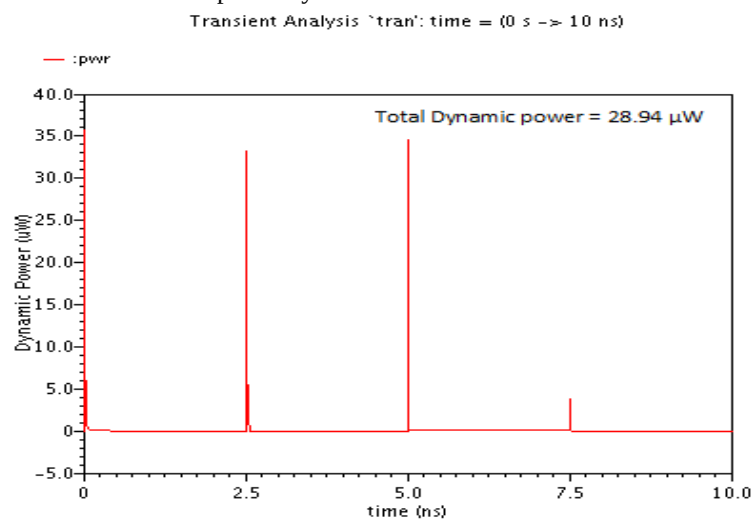


Fig. 5 shows the waveform for total dynamic power in FinFET based 8T SRAM cell

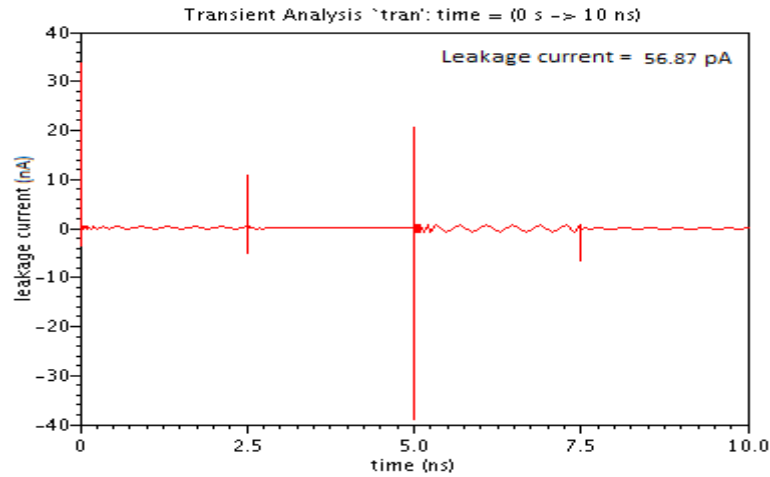


Fig. 6 shows the waveform for total leakage current in FinFET based 8T SRAM cell

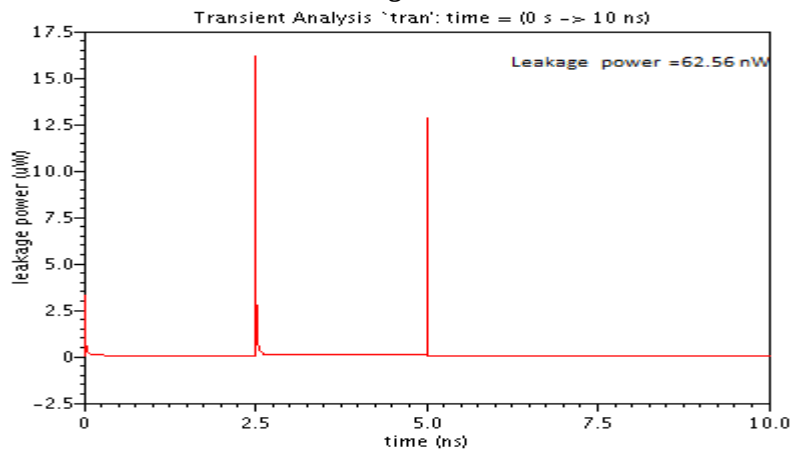


Fig. 7 shows the waveform for total leakage power in FinFET based 8T SRAM cell

Figure 6 and 7 shows the waveform for total leakage current and total leakage power in FinFET based 8T SRAM cell. The total leakage current and total leakage power are $56.87 \times 10^{-12} \text{ A}$ and $62.56 \times 10^{-9} \text{ W}$ respectively. The results obtained from the cadence simulator have been summarized in the table 1. In table 1, we compare the parameters of conventional FinFET based 6T, 7T SRAM cells [10] with FinFET based 8T SRAM cell.

Parameters	FinFET based 6T SRAM cell	FinFET based 7T SRAM cell	Proposed FinFET based 8T SRAM cell
Technology	45nm	45nm	45nm
Supply Voltage	0.7 V	0.7 V	0.7 V
Dynamic Current	$12.34 \times 10^{-5} \text{ A}$	$87.57 \times 10^{-6} \text{ A}$	$41.34 \times 10^{-6} \text{ A}$
Dynamic Power	$8.64 \times 10^{-5} \text{ W}$	$61.31 \times 10^{-6} \text{ W}$	$28.94 \times 10^{-6} \text{ W}$
Leakage Current	$1.79 \times 10^{-9} \text{ A}$	$1.32 \times 10^{-9} \text{ A}$	$56.87 \times 10^{-12} \text{ A}$
Leakage Power	$4.08 \times 10^{-4} \text{ W}$	$2.58 \times 10^{-5} \text{ W}$	$62.56 \times 10^{-9} \text{ W}$

V. CONCLUSION

Analysis of various parameters such as output, dynamic current, leakage current, dynamic power and leakage power of FinFET based 8T SRAM cell has been described in this paper. The analysis of all the parameters has been done using Cadence Virtuoso Tool at 45nm technology. The FinFET based 8T SRAM cell provides better results for dynamic current, dynamic power and improve the leakage current, leakage power as compare to FinFET based 6T and 7T SRAM cells.

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