



Low Power Low Complexity of State Parallel Viterbi Decoder for WiMAX Receiver

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Abstract: A modified state parallel viterbi algorithm referred to as the relaxed adaptive viterbi algorithm that completely eliminates the global best survivor path metric operation possesses great power saving. State parallel VLSI decoder used to develop the relaxed adaptive viterbi decoder by using convolution code decoding to achieve significant power savings and modest area reduction using VHDL coding and synopsys design vision tool for synthesis.

Keywords: VHDL, modelsim, ,synopsis design vision, tool.

I. Introduction

The adaptive Viterbi algorithm, which combines Viterbi algorithm with the principle of T-algorithm which has a computational complexity [1]. This adapts to run-time channel conditions and potential of significant power savings. In contrast to the Viterbi algorithm, the adaptive Viterbi algorithm, winner path at each trellis state does not necessarily become a survivor path, i.e., only those whose path metrics are better than a global non survivor purge limit will be fed to the next decoding depth as survivors. The non-survivor purge limit is determined by the overall best winner path at each decoding depth and varies from one decoding depth to the next. Due to its serial nature, the search-for-the-best-winner operation tends to have a much longer latency than the other operations within the recursive decoding loop. For a VLSI implementation of the adaptive Viterbi algorithm, the long latency due to such a search operation may be concealed by using state-serial decoder architectures or partially state-parallel decoder architecture at the cost of achievable decoding throughput. A configurable state-parallel adaptive Viterbi decoder that can effectively support a large trellis structure but is subject to a relatively long recursive decoding data path[1]. Compared with its state-parallel Viterbi counterpart, a state-parallel relaxed adaptive Viterbi decoder can realize significant power savings and modest area reduction.

The remainder for this paper is organized as follows. Section II and III presents the proposed relaxed viterbi algorithm and design architecture design examples of state parallel relaxed viterbi decoder.

A. Threshold Check

It checks whether at least one survivor has a metric less than threshold value if it is a positive number the output remains high else low [1].

B. Best Branch Metric Search

At the decoding depth, it finds the best (minimum) branch metric, among all the present branch metrics. [1]

C. Branch Metric Normalization

At each depth, given the input which is either zero or real, from the threshold check and the input from the best branch metric Search.[1]

D. Branch Metric Unit

Branch metric unit computes the Euclidean distance between the received convolutions coded symbols and the ideally transmitted symbol. The size of the path metric has strong relations with path metric size.

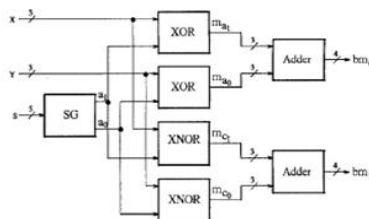


Figure.1 Block Diagram for Branch Metric Unit[6]

Input of the symbol generator is five bit sequence, here symbol generator consists of exor operation shown (1)and(2) as follows.

$$s1 = b0 \oplus b1 \oplus b2 \quad (1)$$

$$s2 = b1 \oplus b2 \oplus b4 \quad (2)$$

Calculation part as shown in below table diagram

TABLE.I Table for symbol generator

INPUT SEQUENCES					OUTPUT	
B0	B1	B2	B3	B4	a0	a1
0	0	1	1	1	1	1
1	0	1	1	0	0	0
1	1	1	0	0	1	1
1	0	1	1	1	0	1
1	1	1	1	1	1	1

II. State Parallel Viterbi Decoder

State parallel viterbi decoder mainly used to decode the convolution codes. Branch metric simply finds the best minimum branch metric path obtained from the trellis structure[1] fed to the best branch metric search unit finds the perfect path between each branches obtained from the trellis structure. Path metrics from source to destination is selected by using butterfly structure in branch metric unit symbol generator is used for generating the generator polynomial sequence and it is given as a input to the exor and exnor gates [6] to get the generated decoded bits here saturated adder is used to combines the branch metrics that are obtained from the symbol generator and exor operation. Branch metric unit output is fed to the branch metric normalization [2]. Add compare and select unit operates in parallel, when decode starts according to the threshold value if the threshold value is positive integer decoding will begin otherwise decoding will not begin. According to the trellis path when decoding process is started the path metrics are initialized to logic low[1]. A feedback signal from add compare select unit deselects the path which doesn't contain Euclidean distance[1]. Survivor memory metric designed by using register exchange based design the validity bits from the ACS units array directly control the clock-gating for power reduction [1]

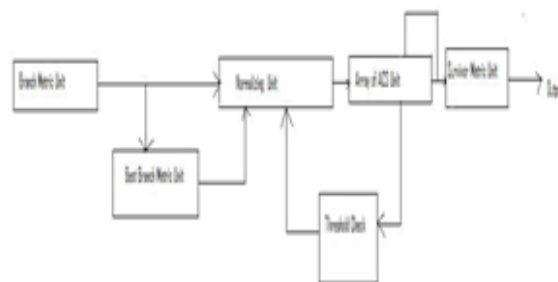


Figure 2 Block Diagram for State-Parallel Viterbi Decoder

III. Results and Discussions

The output wave form for branch metric unit with the metrics consists of 3 bit binary sequence as shown in figure.6

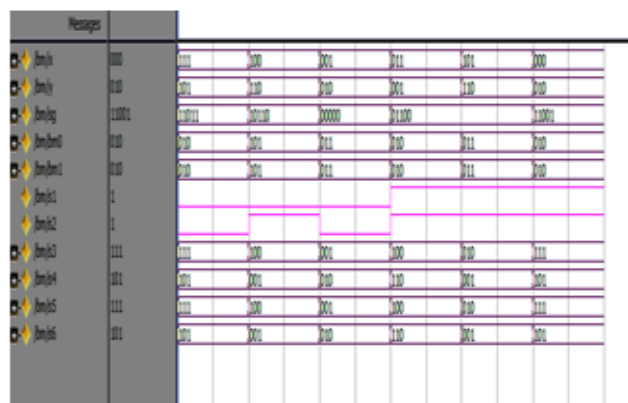


Figure 3 Output wave form for Branch Metric Unit

TABLE.III State Table for state Parallel viterbi decoder for branch metric unit

States	Input sequence	Input	Next state	Output	
			m0 m1 m2	V0	V1
a)	000	0	a) 0 0 0	0	1
		1	e) 1 0 0	1	0
b)	001	0	a) 0 0 0	0	0
		1	e) 1 0 0	1	0
c)	010	0	b) 0 0 1	1	1
		1	f) 1 0 1	0	1
d)	011	0	b) 0 0 1	1	1
		1	f) 1 0 1	0	1
e)	100	0	c) 0 1 0	1	1
		1	g) 1 1 0	0	1
f)	101	0	c) 0 1 0	1	1
		1	g) 1 1 0	0	1
g)	110	0	d) 0 1 1	0	0
		1	h) 1 1 1	1	0
h)	111	0	d) 0 1 1	0	0
		1	h) 1 1 1	1	0

The output wave form for state parallel viterbi Decoder for WiMax receiver reset, clock or clk'event then the output is changes from current state to next state that is if the input is high clock is low to high and reset is logic low then current state s0 is change to next state s5 according to the input sequence current and next state is depends shown in figure.7

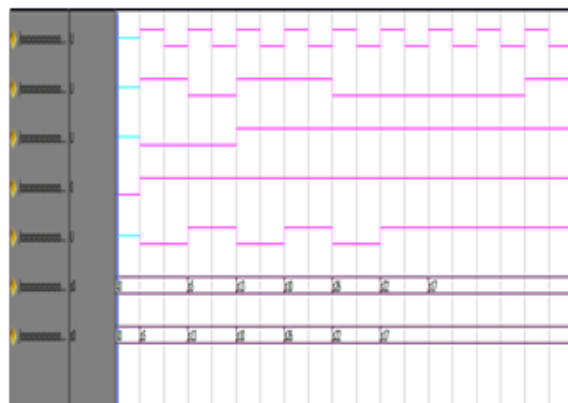


Figure 4 Output wave form for Wimax Receiver using state parallel viterbi decoder

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Library(s) Used:

lsl_10k (File: /Synopsys/Tools/syn_v8-2008.09-SP1/libraries/syn/lsl_10k.db)

Information: The cells in your design are not characterized for internal power. (PWR-223)

Operating Conditions:
Wire Load Model Node: top

Global Operating Voltage = 5
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 0.100000ff
Time Units = 1ns
Dynamic Power Units = 100nW (derived from V,C,T units)
Leakage Power Units = Unknown

Cell Internal Power = 0.0000 uW (0%)
Net Switching Power = 3.7068 uW (100%)
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Total Dynamic Power = 3.7068 uW (100%)
Cell Leakage Power = 0.0000

1
design vision

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Figure5 Power Report for State Parallel Viterbi Decoder

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*****
Report : area
Design : 0000000000000000
Version: B-2008.09-SP3
Date   : Thu Sep 30 23:58:12 2010
*****

Library(s) Used:

    lsi_10k (File: /Synopsys/Tools/syn_vB-2008.09-SP3/libraries/syn/lsi_10k.db)

Number of ports:      5
Number of nets:       94
Number of cells:      86
Number of references: 15

Combinational area:   125.000000
Noncombinational area: 50.000000
Net Interconnect area: undefined (No wire load specified)

Total cell area:      175.000000

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Figure6 Area Report for State Parallel Viterbi Decoder

V. Conclusion

State parallel viterbi decoder is used for fast decoding sequence rather than relaxed adaptive decoder. Switching activity is reduced by using half rate convolution code by using VHDL coding and synthesis done by using synopsys design vision tool. Less area and power consumption in state parallel viterbi decoder

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