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Performance Analysis of Low Power Dissipation and High Speed Voltage Sense Amplifier

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Abstract: This CMOS voltage sense amplifier or comparator is designed by adding dual input single output differential amplifier which is added in place of back-to-back inverter in the latch stage. This method is used to completely remove the input noise present in the circuit. Using this dual input single output differential amplifier the analog-to-digital conversions with high speed, lower power dissipation and immune to noise can be achieved. The circuits are designed using 180nm Technology and CMOS at a power supply of 1.8 Volts in Cadence. This proposed single output differential amplifier is based on two cross coupled differential pairs with positive feedback and switchable current sources and having lower power dissipation, higher speed and it is shown to be very robust against transistor mismatch and is noise immunity. There is a reduction of 24% in the delay of the circuit and also the energy consumed in the circuit is only 77% of the previous circuit and hence there is an increase in speed and decrease in the dissipation of the circuit.

Keywords: CMOS, differential amplifier, energy, mismatch, analog to digital converter

I. Introduction

High-speed voltage sense amplifiers are essential building blocks in high-speed flash analog-to-digital converters (ADCs). Such ADCs are widely used in many applications including data storage systems, fast serial links and high-speed measurement instruments. In these applications, typically a low-to-medium resolution ADC (i.e., 4 to 6 bits of resolution) and speeds of the order of GHz are desired [1]. In voltage sense amplifiers first the input signal is sampled. Then the sampled signal is applied to a number of comparators to determine the digital equivalent of the analog value. The voltage sense amplifiers are applied to read the contents of several types of memories and also to compare the inputs and giving the result accordingly. Apart from that, voltage sense amplifiers are used in peak detectors, zero crossing detectors, switching power regulators.

Nowadays high speed devices like High speed ADCs, operational amplifiers became of great importance. And for these high speed applications, a major thrust is given towards low power methodologies. They can be thought of as decision making circuits. Minimization in power consumption in these devices can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non idealities will greatly affect the overall performance of the device. Now analog-to-digital converter requires lesser power dissipation, low noise, better slew rate, high speed, less hysteresis, less Offset. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and voltage sense amplifiers. The power consumption, speed takes major roll on performance measurement of ADCs.

Dynamic voltage sense amplifiers are being used in today's A/D converters extensively because these comparators are high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise [2]. But this stage based comparator have disadvantage of more power consumption due to the presence of more number of transistors and also the reduction in intrinsic gain due to the reduction of the resistance because of continuous technology scaling [5].

The organization of the rest of the sections of the paper is as follows. In the next section we will be analyzing the voltage sense amplifier circuit and in the III section we will be comparing the results and then will be followed by conclusion and references. The simulation graphs are also being attached along with the schematic of the circuit.

II. Analysis of Comparators

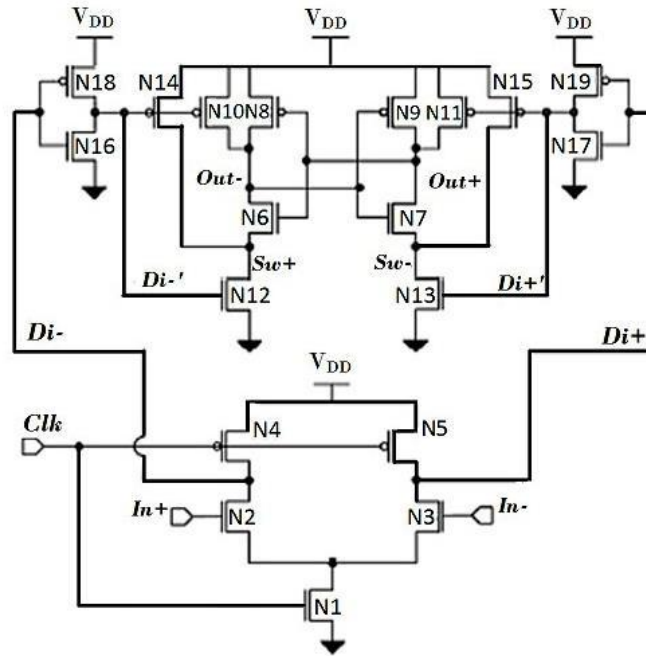


Figure 1: Circuit with back-to-back inverters

The circuit-2 mainly is a derived version of the circuit-1 shown above. The back-to-back latch stage is replaced with back-to-back dual input single output differential amplifier. This Differential amplifier stage is having many advantages over the latch stage. These are having low common noise because of the presence of the additional nmos and also they are more immune to the environmental noise. Because of the presence of this stage the achievable voltage swing also increases. It also provides simpler biasing and higher linearity. The delay of the circuit also reduces due to this structure and also the consumption of the circuit reduces. Here our main purpose is to eliminating the noise that is present in the latch stage and for which output is getting fluctuated with clock transition.

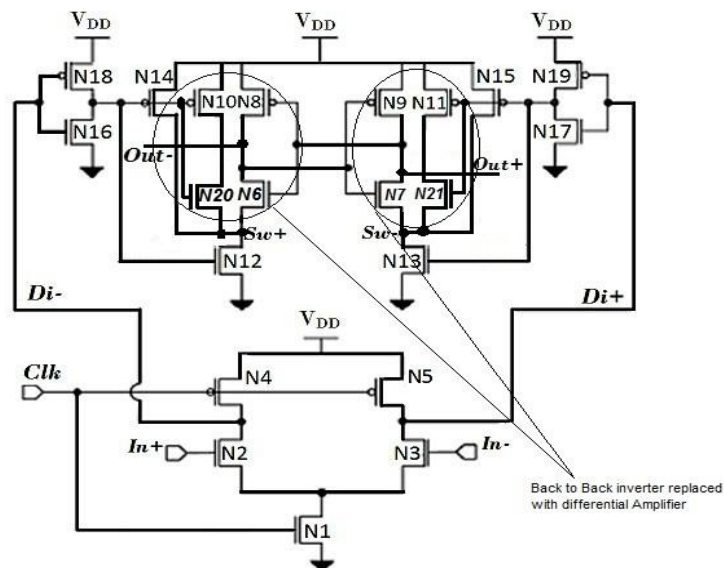


Figure 2: Modified circuit with differential amplifier

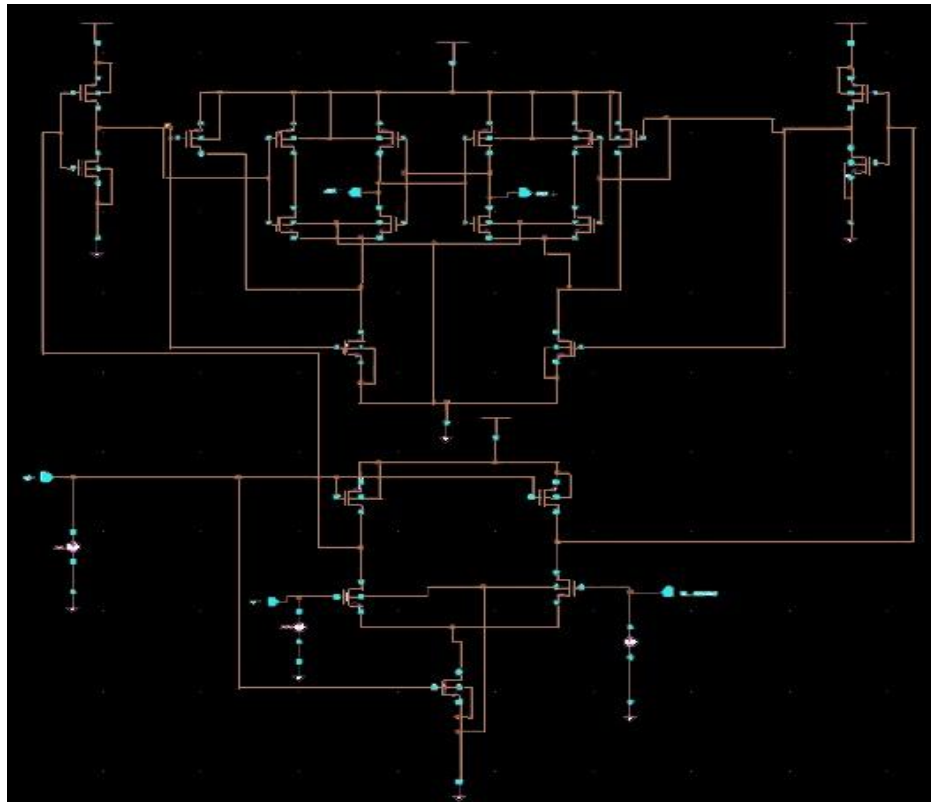


Figure 3: Cadence implementation of the modified circuit

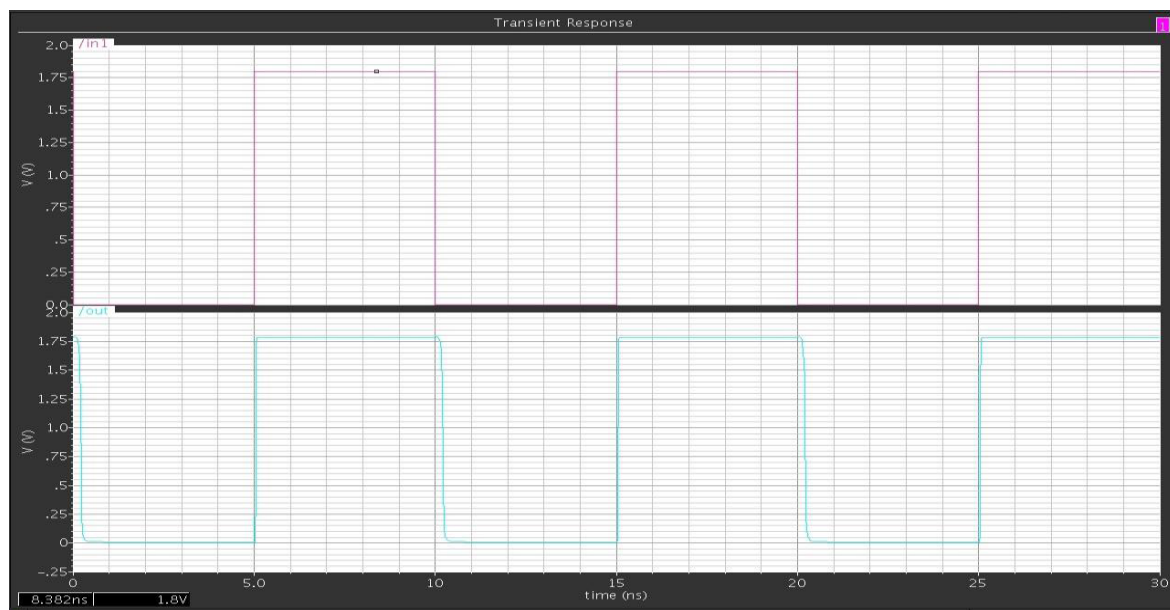


Figure 4: The waveforms of the input and corresponding output

Firstly we will discuss the working on the circuit. During reset phase ($\text{clk} = 0\text{V}$), PMOS transistor N4 and N5 turn on and they charge Di node voltages to VDD and Hence NMOS transistors N16 and N17 turns on and discharges Di' nodes voltages to GND. Then N14, N15 and PMOS transistors of differential amplifier blocks N10 and N11 turns on, NMOS transistors of differential amplifier block N6, N7 and N12, N13 turns off. The out nodes are charges to VDD.

During evaluation phase ($\text{clk} = \text{VDD}$), the Di node capacitances are discharged from VDD to GND in a rate which is proportional to the input voltages. At a certain voltage of Di nodes, the inverter pairs N18/N16 and N19/N17 invert the Di node signal into a regenerated signal. These regenerated signals turn PMOS transistors N14, N10, N11, and N15 off. And eventually N12, N13, N20, N21 turns on. Hence the back-to-back differential

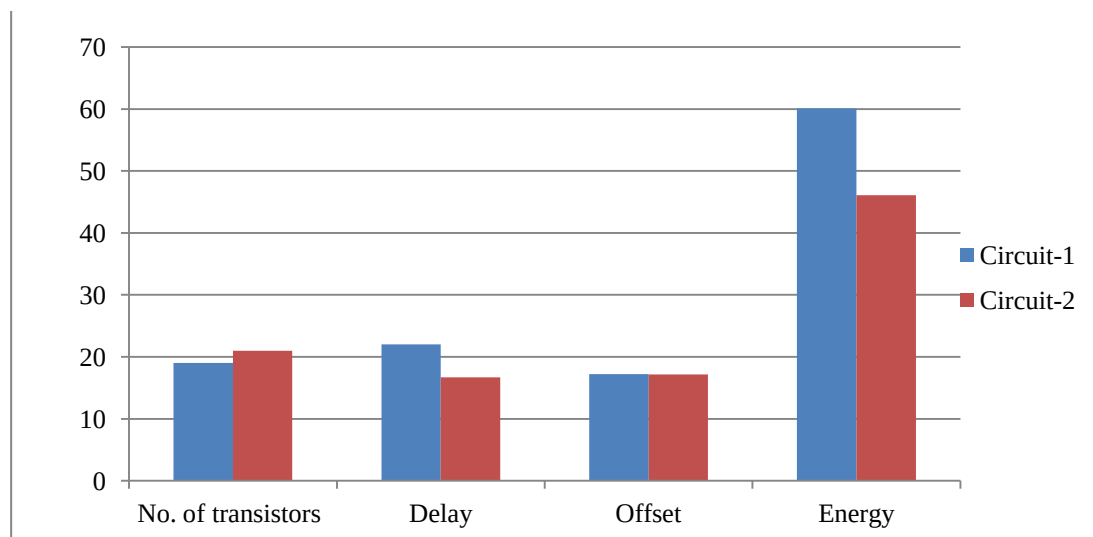
pair again regenerates the Di' node signals and because of N12 and N13 being on, the output latch stage converts the small voltage difference transmitted from Di' node into a full scale digital level output.

III. Comparison of the results with previous work

We have done the analysis of the circuit for calculating the delay, offset voltage and energy. The software used for circuit designing and simulation is Cadence Analog Suite (Virtuoso) at 180nm CMOS Technology (VDD=2V and common mode Voltage Vcom=1.8V). The results table is shown below by which we can clearly see that the delay of the circuit has been reduced and also the energy consumed by the circuit has been decreased while there is no change in the offset voltage of the voltage sense amplifier. The results of the circuit-1 are taken from[3].

Table 1: Performance Comparison

	No. of transistors	Delay(pS)	Offset voltage(mV)	Energy (fJ)
Circuit-1	19	22	17.2	60.08
Circuit-2	21	16.7	17.2	46.1



IV. Conclusion

The paper presents the low power voltage sense amplifier which is having a lower delay in comparison to the previous circuit by the addition of differential amplifiers. The circuit has approximately 24% reduction in delay factor in comparison to the circuit which was having inverters and the energy consumed in the circuit is also approximately 77% of the previous work.

VI. References

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