

Design and Analysis of High Speed SRAM Cell at 45nm Technology

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Abstract: SRAM often faces the problem of read stability due to static noise while reading, as the basic latch is accessed by the access transistors which may cause external noise to corrupt the stored data. The aim of this paper is to analyze the read behaviour of the multiple SRAM cell structures using cadence tool at 45nm technology and to compare the cells for read operation while keeping the read and write access time and the supply voltage as low as possible. While the conventional 6T cell utilizes the same word line for read as well as write access, the new cell structures described in this paper use a different read enable line for read operation. This allows the memory element to remain isolated from any disturbance due to bit-lines or access transistors.

Keyword: SRAM cell, High speed, Read Stability, Low Power.

I. INTRODUCTION

The SRAM topology proposed in this paper uses multiple 10T structure to produce a faster read operation without disturbing the cell [1]. In conventional 6T SRAM, the read operation is performed by pulling the word line high and accessing the latch by access transistors. This may lead to disturbance and corruption of the data stored in the cell, due to static noise. Further, in conventional 6T cell, the read operation is quite slow process as activating the access transistors takes undesirable time to access the latch. Slow read operation in SRAM means time required to respond to a particular operation (read or write) would be large. As a result, the leakage power over this long period of time in the idle circuit would increase. This reduces the performance of the cell and makes the cell objectionable for use in the practical applications. The circuit is thus expected to respond as fast as possible and to be switched OFF after the response has been observed. However in case of SRAMs, switching OFF the circuit would lose the data, and regrettably it is a compulsion to keep the cell ON even if it is in idle state. This situation becomes a major challenge to reduce the leakage current as we have no option but to keep the circuit ON. To overcome the limitations mentioned above, the proposed SRAM cell has been equipped with a different read process which limits the time required to read the cell and helps in prohibiting the data corruption of cell by isolating it from the external read circuitry. The cell has been designed to work with lower supply voltages, which helps in further degradation of the leakage power thus making the cell more efficient.

II. LIMITATIONS OF 6T CELL

In conventional 6T cell, as shown in figure 1, the memory element is accessed for read operations using access transistors. This leads in undesired delay to activate the access transistors and then sensing the bit lines.

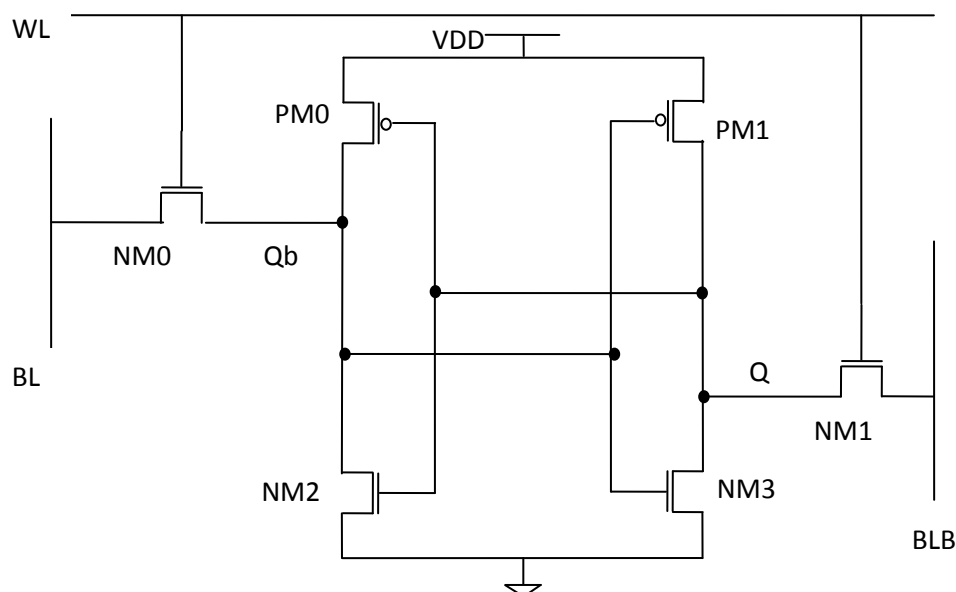


Figure 1. The Conventional 6T SRAM Cell.

the write speed of the cell would still be slow which leads to degradation of write speed performance of the cell. The write waveform of the 10T structure is shown in figure 3 and read waveform in figure 4.

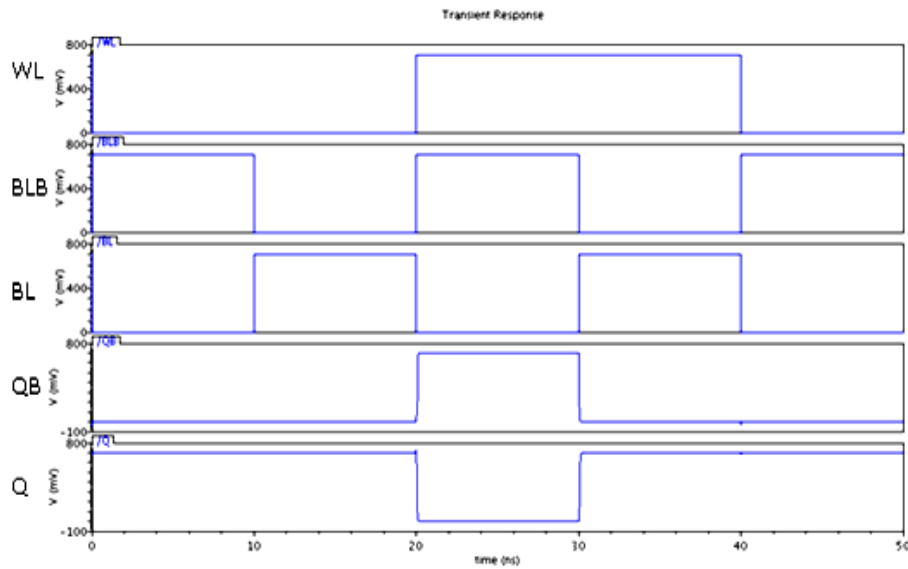


Figure 3. Waveform for write operation of 10T SRAM Cell.

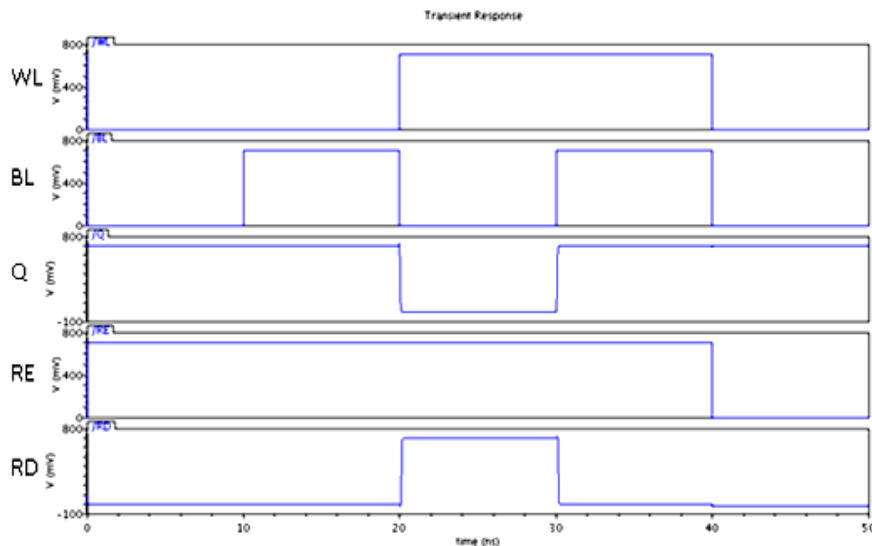


Figure 4. Waveform of read operation of 10T SRAM Cell.

According to the write waveform, Q and QBar (QB) depend on Bit Line (BL) and Bit Line Bar (BLB) respectively. When write line (WL) is at high voltage (say, 1 V) then output Q depends on BL and QB depends upon BLB. The write 1 delay, 120 ps, is less than the write 0 delay 110 ps in revealed waveforms.

According to read waveform, as the inverter is connected directly with memory element before the access transistor to make the read operation independent on access transistors and buffer is connected to inverter output consequently the read buffer is connected to circuit for robust and fast read operation at low voltage. The read output depends on read enable (RE) and read enable bar (REB) which are kept at opposite voltages. The interval at which both WL and RE are high, the read will occur. Hence the circuit becomes independent of bit lines and gives disturb free read operation. The read delay in the circuit is 50 ps.

IV. POWER CONSUMPTION

Power consumed in any circuit can be due to a number of parameters like sub-threshold leakage, temperature and also at larger supply voltage (V_{dd}) [7] [9] [12]. The 6T SRAM Cell, has more sub-threshold leakage as compared to 10T SRAM Cell due to read-disturb free circuit. The disturb-free read circuit, connected to output node Q before access transistor, reduces the delay and leakage throughout the read cycle since the circuit becomes independent of access transistors and hence does not depend on bit lines.

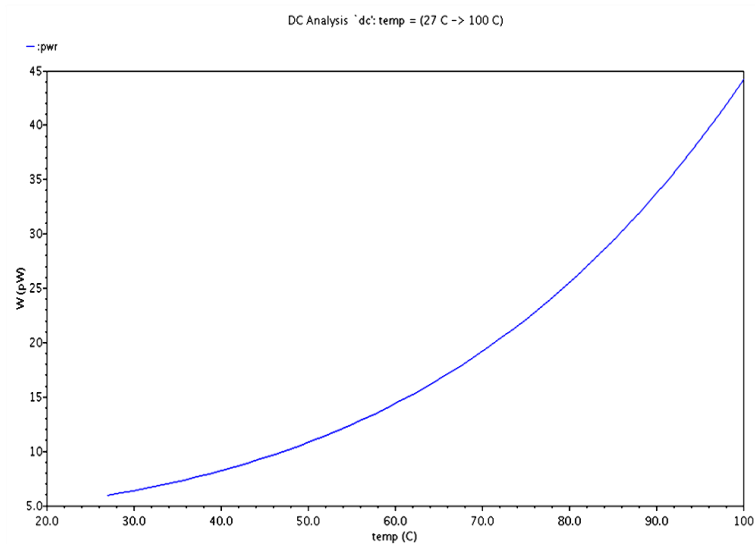


Figure 5. Power versus temperature curve of 10T Cell.

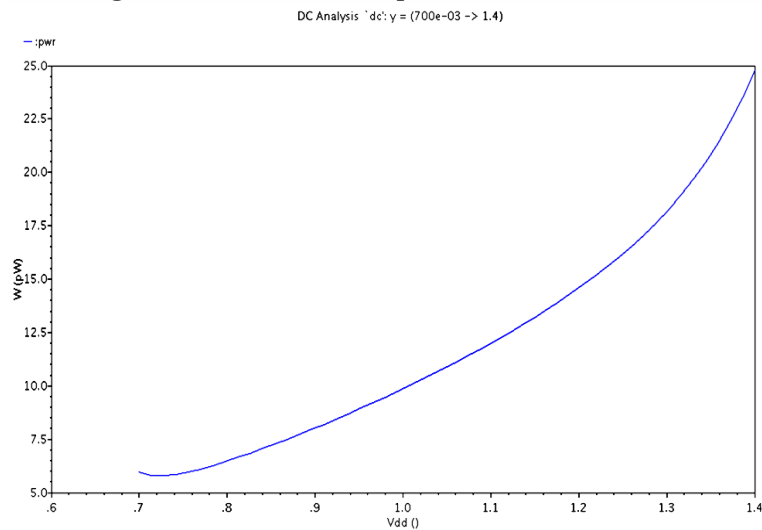


Figure 6. Power versus Vdd curve of 10T Cell.

During the read cycle high voltage is stored at node Q, the transistor NM4 shows the leakage since it becomes off. Variation of power consumption with respect to temperature and supply voltage is plotted in figure 5 and figure 6 respectively. The overall circuit leakage power is reduced to 19.09 nW. The leakage power waveform is shown in figure 7.

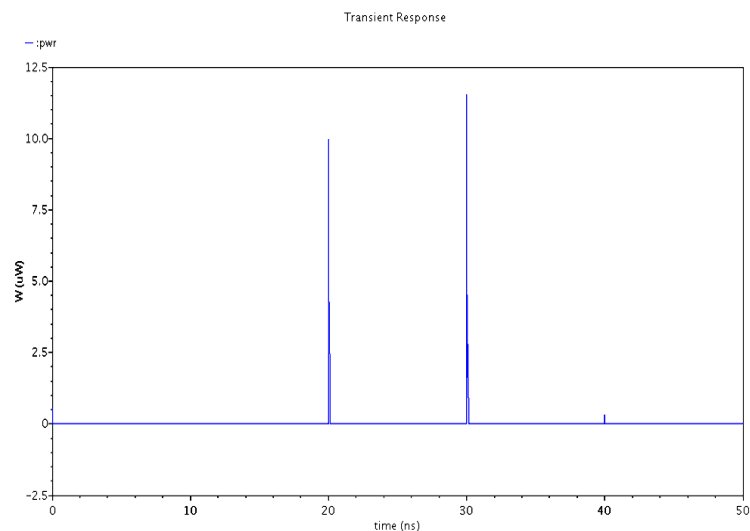


Figure 7. Leakage power waveform of 10T SRAM Cell.

V.SIMULATION RESULTS

The simulation of the 10T SRAM cell is performed with Cadence virtuoso tool at 45 nm technology. Calculation of different parameters is summarized in table 1. Results show that delay is improved to 13% and power has been reduced up to 36% with disturb-free read operation. The most important observation of this cell is that the read delay operation has been reduced up to 54% which can be clearly observed from table 1, thus making the read operation very fast.

Table 1: Simulation Results as obtained from cadence.

Sr.No.	Parameter	6T Cell	10T Cell
1	Technology	45nm	45nm
2	Power	19.09 nW	12.09 nW
3	Write 1 Delay	138 ps	120 ps
4	Write 0 Delay	135 ps	110 ps
5	Read Delay	110 ps	50 ps
6	Supply Voltage	700 mV	700 mV

VI.CONCLUSION

As the paper was aimed at the analysis of high speed cell, we conclude that 10T SRAM, equipped with read-disturb free circuit has shown improved read delay performance thus increasing the SNM of the cell. Results, therefore confirm that 10T SRAM cell would be a better choice as compared to 6T cell to be employed in the practical circuits.

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