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Ultra Low Power High Speed MAC Unit Using LP-HS Logic in CMOS Technologies

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Abstract: A modified approach for constant delay logic style is developed in this paper to provide improved power and delay named LP-HS logic. Constant delay logic style is examined against the LP-HS logic, by analysis through simulation. It is shown that the proposed LP-HS logic has low power, delay and power delay product over the existing constant delay logic style. Multiplier accumulator unit is one of the important applications in DSP. In this paper the comparison of MAC using both constant delay logic style as well as LP-HS logic have been done. The simulation results shows that MAC using LP-HS logic is better in terms of power, delay and power delay product when compared to constant delay logic style. The simulations were done using HSPICE tool in 45nm, 32nm, 22nm and 16nm CMOS technologies and performance parameters of power, delay and power delay product were compared.

Keywords: CMOS, MOSFET, VLSI, Power Consumption, Delay, Power delay product (PDP), Constant Delay Logic (CD logic)

I. Introduction

High performance energy efficient logic style is always important in VLSI circuits. CMOS is the most dominant technology which is used to construct these types of integrated circuits. The most widely accepted parameters to measure the quality of a circuit or to compare various circuit styles are power, delay and area. Advances in CMOS technology have led to improvement in the performance in terms of power, delay and area. There always exists a trade-off between power, delay and area in a circuit. The power delay product is a figure of merit for comparing logic circuit technologies or families. [2] The two different families in the logic style are the static logic and dynamic logic. [5][6] Static CMOS is the widely used logic style which consists of pull down network (PDN) and pull up network (PUN). It is truly an extension of the static CMOS inverter with multiple inputs. This logic is static because 1 and 0 are restored by pull up and pull down network respectively. This type of design is having high functional reliability and is very easy to design. Requirement of large implementation area is the major disadvantage of this technique. [1]

Despite its advantages static CMOS suffers from increased area, and correspondingly increased capacitance and delay. Thus we go for pseudo nMOS logic. It is a ratioed logic. The major advantage of this technique is the low area cost which in turn low input gate load capacitance. These forms are not meant to replace complementary CMOS but rather to be used in special applications for some particular purposes. The major drawback of this technique is the non-zero static power dissipation. Even though pseudo nMOS logic is having many advantages, because of its static power dissipation we go for dynamic logic. Dynamic logic uses a special technique called dynamic precharging. [12] Normally during the time the output is being precharged, the nMOS network should not be conducting. This is usually not possible. Because of the disadvantage of the above logic a new type of dynamic logic called the precharge-evaluation logic is proposed. The drawback of this logic is the charge leakage, charge sharing and cascading problem. Monotonicity problem also exists in case of dynamic logic. [7] In order to mitigate the problems of the dynamic logic several modifications for the existing dynamic logic is made which leads to the introduction of CMOS domino logic, self timed domino logic, NORA domino (NP CMOS) etc.

In order to eliminate the problems associated with the domino logic a new type of logic called feedthrough logic has been introduced. [4][8][9] Basic feedthrough logic is modified in many ways to get rid of the drawbacks associated with them. A new type of feedthrough logic called dynamic feedthrough logic has also been introduced. [10][11][13] To mitigate the problems associated with the feedthrough logic (FTL) a new high performance logic known as constant delay logic style has been designed. This high performance energy efficient logic style has been used to implement complicated logic expressions. In this paper some modifications have been done for the constant delay logic style to reduce the power consumption and to improve the speed. The proposed technique is known as the LP-HS logic.

II. Constant Delay Logic Style

Designers of digital circuits often desire fastest performance. This means that the circuit needs high clock frequency. Due to the continuous demand of increase operating frequency, energy efficient logic style is always

important in VLSI. One of the efficient logics which come under CMOS dynamic domino logic is the feedthrough logic (FTL). Dynamic logic circuits are important as it provides better speed and has lesser transistor requirement when compared to static CMOS logic circuits. Feedthrough logic has low dynamic power consumption and lesser delay when compared to other dynamic logic styles.

To mitigate the problems associated with the feedthrough logic new high performance logic known as constant delay (CD) logic style has been designed.[3] It outperforms other logic styles with better energy efficiency. This high performance energy efficient logic style has been used to implement complicated logic expressions. It exhibits a unique characteristic where the output is pre-evaluated before the input from the preceding stage is ready. Constant delay logic style which is used for high speed applications is shown in Fig 1.

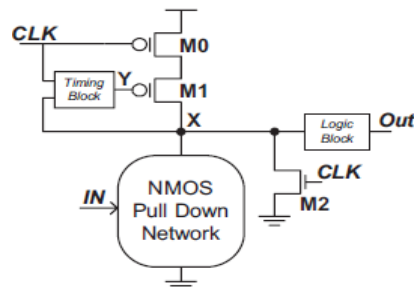


Fig 1: Constant Delay Logic Style [3]

CD logic consists of two extra blocks when compared to feedthrough logic. They are the timing block (TB) as well as the logic block (LB). Timing block consists of self reset technique and window adjustment technique. This enables robust logic operation with lower power consumption and higher speed. Logic block reduces the unwanted glitch and also makes cascading CD logic feasible. The unique characteristic of this logic is that the output is pre-evaluated before the inputs from the preceding stage got ready. An Nmos pull down network is placed where the inputs are given. Based on the logic which is given in the pull down network we will get the corresponding output. A buffer circuit implemented using CD logic is shown below. The expanded diagram for timing block as well as logic block is also shown in the Fig 2

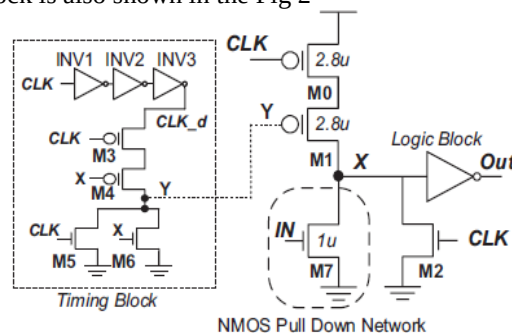


Fig 2: Buffer Using CD Logic [3]

The chain of inverters is acting as the local window technique and the NOR gate as a self reset circuit. Length of the inverter chain varies according to the circuit which we have to design. The prime aim of the inverter chain is to provide a delayed clock. The contention problem which is one of the disadvantages of the feedthrough logic is reduced with the help of this window adjustment. In the self reset circuit one of the input of the NOR gate is the intermediate output node X and the other one is the clock. The logic block is simply a static inverter as in the case of dynamic domino logic. Since the above circuit is for a buffer the NMOS pull down network consists of only one nMOS transistor.

The timing diagram for constant delay logic is shown in Fig 3. CD logic works under two modes of operation.

- i. Predischage mode (CLK=1)
- ii. Evaluation mode (CLK=0)

Predischage mode happens when CLK is high and evaluation mode occurs when CLK is low. During predischage mode X and Out are predischarged and precharged to GND and VDD respectively. During evaluation mode three different conditions namely contention, C-Q delay and D-Q delay takes place in the CD logic. Contention mode happens when IN=1 for the entire evaluation period. During this time a direct path current flows from pMOS to PDN. X rises to nonzero voltage level and Out experiences a temporary glitch. C-Q delay (clock-out) occurs when IN goes to 0 before CLK transits to low. At this time X rises to logic 1 and Out is discharged to VDD and the delay is measured from CLK to Out. D-Q delay happens when IN goes to 0 after CLK transits to low. During this time X initially enters contention mode and later rises to logic 1 and the delay is measured from IN to Out.

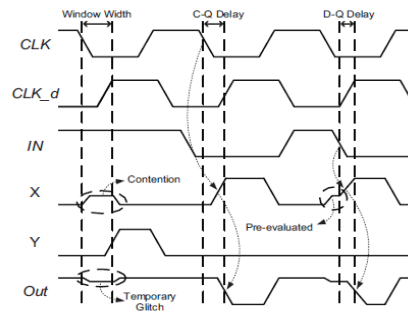


Fig 3: Timing Diagram of CD Logic [3]

III. Proposed LP - HS Logic

The proposed LP-HS logic is derived from the existing constant delay logic. When compared to CD logic there are three major differences in the LP-HS logic. The window adjustment technique is eliminated in this logic. The evaluation transistor is altered as pMOS transistor instead of nMOS. The third variation is the addition of the transistors M2 and M3 in parallel below the pull down network. The proposed logic helps to reduce the power and delay which in turn reduces the power delay product. The circuit diagram for the proposed logic is shown in Fig 4

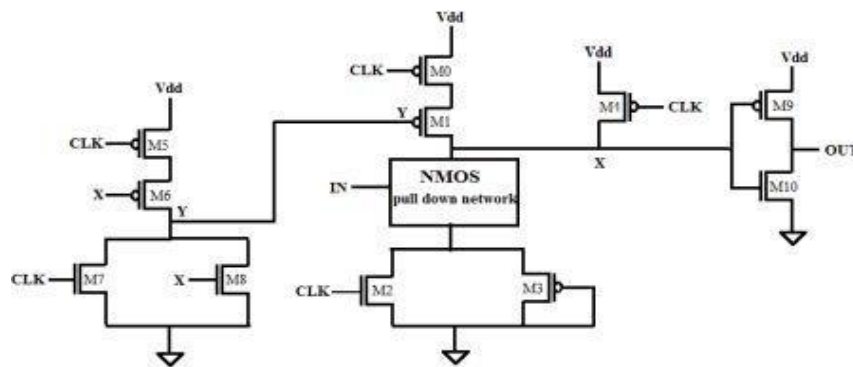


Fig 4: Proposed LP-HS Logic

Transistors M0 and M1 whose gates are driven by the CLK and the output of NOR gate are connected in series. This increases the resistance which in turn helps reducing the power. M4 is acting as an evaluation transistor. The NOR gate which is behaving as the self resetting logic is constituted by the transistors M5, M6, M7 and M8. M5, M6 and M7, M8 is driven by CLK and the output intermediate node X. IN values are given to the nMOS pull down network which is given according to the circuit which we have to design. Transistors M2 and M3 are connected in parallel and is placed down to the nMOS pull down network. These transistors help to reduce the power delay product. The gate of M2 is driven by the clock and M3 is at ground. Transistor M2 increases the dynamic resistance of the pull down network which successively helps to reduce the power consumption. Transistors M9 and M10 together figures the static inverter which is used to make the cascading logic more feasible.

The circuit works under two modes of operation.

- i. Precharge mode (CLK=0)
- ii. Evaluation mode (CLK=1)

Precharge mode occurs when clock is low and evaluation mode happens when clock is high. When clock is low, transistor M4 gets ON and provides a high value at node X which in turn provides a low value at the output node OUT. When clock is high the transistor M2 gets ON and the nMOS pull down network is evaluated and gives the output. During this time the transistor M0 whose gate is driven by the CLK is in OFF condition. Due to this the contention mode gets wiped out in the evaluation condition which in turn tends for the elimination of window adjustment technique in the proposed logic. One of the reasons for the power and delay reduction in the circuit is the elimination of the window adjustment technique. During the evaluation mode the pull down network and the transistor M2 gets ON which provides high dynamic resistance which further reduces the power. Transistor M3 is in always ON condition which offers an easy discharge of the value to the ground.

IV. Existing MAC Unit

High speed and low power multiplier accumulator unit is utmost requirement of today's VLSI systems and digital signal processing applications like FET, Finite impulse response filters, and convolution etc. These applications require the computation of the sum of products of a series of successive multiplications. [10] In order to implement such functions this special unit called multiplier accumulator is required. A MAC consists of

a multiplier, adder and a special register called accumulator. A basic MAC unit is shown in Fig 5. Basically a MAC unit employs a fast multiplier fitted in the data path and the multiplied output of multiplier is fed into a fast adder which is set to zero initially.[8] The result of addition is stored in an accumulation register. The MAC unit should be able to produce output in one clock cycle and the new result of addition is added to the previous one and stored in the accumulator register. It is capable of multiplying and adding with previous product consecutively. [11] The equation for MAC operation is given as

$$a = a + (b \times c)$$

where a is the accumulator register, b is the multiplier and c is the multiplicand.

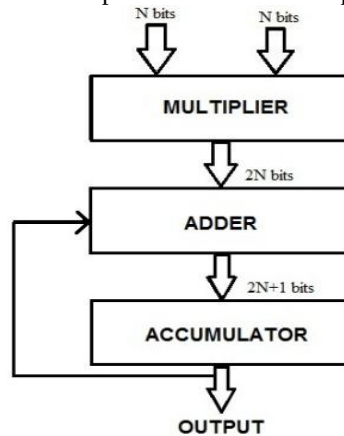


Fig 5: Basic MAC Unit

V. MAC Unit Using LP-HS Logic

Digital Signal Processing (DSP) is the application of mathematical operations to digitally represent signals. DSP processors share basic features designed to support high-performance, repetitive, numerically intensive tasks. MAC is the most important block in DSP system. The goal of this proposed multiplier accumulator unit is to use for digital signal processing applications. It is capable of multiplying and adding with previous product consecutively. Fig 10 depicts the block diagram of the proposed multiplier accumulator unit. This MAC design is composed of a 4 bit Wallace tree multiplier, 8 bit ripple carry adder and a 9 bit parallel in parallel out shift register designed using reset D flip flop.

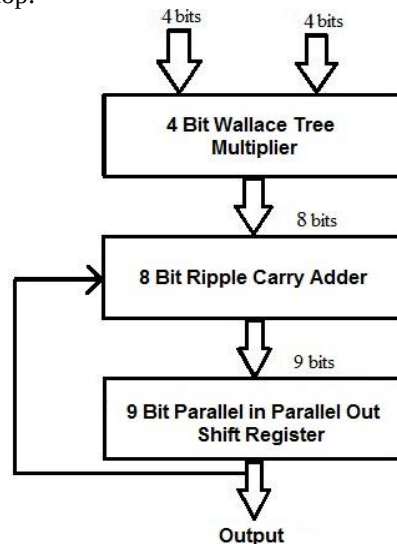


Fig 10: Block Diagram of Proposed MAC Unit

The two 4 bit inputs for the MAC are fed to the 4 bit Wallace tree multiplier block of the MAC. It generates 8 bits at the output which is then fed to the 8 bit ripple carry adder block. The layout of this adder is simple which allows for fast design time. The 9 bit parallel in parallel out shift register is used as the accumulator whose initial values are set to 0 with the help of reset pin. The output of the PIPO is then sent to the 8 bit ripple carry adder. This MAC unit has 9 bit output and its operation is to add repeatedly the multiplication results. Apparently, together with the utilization of Wallace tree multiplier approach, ripple carry adder as the adder and PIPO shift register as the accumulator, this MAC design can enhance the MAC unit speed and reduces the power consumption so as to gain better system performance.

VI. Performance Analysis

Here the performance analysis like power, delay and power delay product of multiplier accumulator unit using CD logic as well as LP-HS logic have been carried out using HSPICE tool and there results were compared and is shown in the table below.

Table 1: Power, Delay and PDP analysis of MAC Unit in different nanometer technologies

TECHNOLOGY	CD LOGIC			LP – HS LOGIC		
	Power (µw)	Delay (ps)	PDP (fJ)	Power (µw)	Delay (ps)	PDP (fJ)
45nm	175.40	74.39	13.04	19.63	68.84	1.35
32nm	114.80	68.61	7.88	13.90	60.82	0.85
22nm	180.20	43.49	7.84	11.87	35.89	0.45
16nm	19.46	75.23	1.46	2.69	53.71	0.14

VII. Conclusion

New high performance LP-HS logic has been proposed. The Multiplier Accumulator Unit is designed using existing and proposed logic. It is simulated with 45nm, 32nm, 22nm and 16nm CMOS technologies and the performance parameters power, delay, power delay product were compared. The simulations for 45nm, 32nm and 22nm CMOS technologies were carried out at 0.9 V, while 16nm CMOS technology was simulated at 0.6V. The operating frequency for all the technologies was kept at 1GHz. From the results it is found that the power delay product has been improved by 89.64% for the multiplier accumulator unit using the proposed logic in 45nm CMOS technology. A betterment of 89.21% has been found for the multiplier accumulator unit using the proposed logic for 32nm CMOS technology. Similarly an improvement of 94.26% and 90.41 % were found for the proposed multiplier accumulator unit in 22nm CMOS technology and 16nm CMOS technology respectively.

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