



International Journal of Emerging Technologies in Computational and Applied Sciences (IJETCAS)

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Review on different types of Junctionless Transistors

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Abstract: In this paper review study on different types of Junctionless transistor is promoted. Here a comparative study of SOI, bulk planar, double gate and tunnel Junctionless field effect transistor. It is observed Junctionless transistor exhibits better short channel effects and ON current then inversion mode device. Tunnel Junctionless transistor exhibits the properties of both tunnel FET and Junctionless transistor

Keywords: Junctionless, bulk planar, Tunnel Junctionless, SOI, double gate.

I. Introduction

Fundamental building block of all the modern electronic device are transistor. The down scaling of transistor results in significant challenges in manufacturing process and need of new device structure [1]. PN junctions are commonly present in all MOS transistor in their drain and source junction. PN junction is formed by making contact of silicon which is doped with trivalent impurity in one side and pentavalent impurity in the other side. There are also junctions like Schottky junction [2] having metal and semiconductor contact, heterojunction which contain two different semiconductor material [2]. Depending on the bias applied the junction will allow or block current flow through it. MOSFET and BJT contains two PN junction, JFET contains only one PN junction and schottky junction is present in MESFET. The distance between the source and drain junction gives effective channel length in MOSFET.[1] The region between source and drain have opposite doping with respect to source and drain doping. As the transistor junctions are scaled down to 10 nm it requires extremely high doping concentration, low thermal budget processing, flash annealing technique. So to overcome these challenges we go for accumulation mode devices which have same doping at channel, drain and source. SOI structures using accumulation mode technology have already been realized in Omega-gate FETs[3], FinFETs[4], Gate-all-Around FETs[5] Pi-gate FETs [6] and Multigate FETs[7]. P-channel and N-channel device have a P+-P-P+ and N+-N-N+ doping profile for source, channel and drain.

A new device structure based on Lilienfeld's first transistor architecture [8] which don't have any junction has been proposed and fabricated called the Junctionless transistor. The Lilienfeld's transistor is a field effect device, substantial like modern metal-oxide-semiconductor (MOS) devices. It consists of a thin semiconductor film placed on a thin insulator layer, itself deposited on a metal electrode. The latter metal electrode serves as the gate of the device. In operation, the current flows in the resistor between two contact electrodes, in much the same way that drain current flows between the source and drain in a modern MOSFET[9]. The Lilienfeld's device is a simple resistor, and the application of a gate voltage allows the semiconductor film of carriers to be depleted, thereby modulating its conductivity [1]. Ideally, it should be possible to completely deplete the semiconductor film of carriers, in which the resistance of the device becomes quasi-infinite. The Junctionless transistor is an accumulation mode device with no PN junctions in the vertical direction, the source, drain and channel have same doping concentration. It is basically a gated resistor where the carrier mobility in the device is controlled by the gate. During ON state it has large current due to high doping concentration of the channel region.[10] In OFF state the carrier are depleted due to the work function difference between the semiconductor and the gate material. The cross sectional area of the device should be small so that the carriers can be depleted during OFF state. As a result very low OFF current is achieved. The ON current is dependent on doping concentration where as in MOSFET it is dependent on gate capacitance [11].

Different Junctionless architecture are available in the literature [1], [9]-[38] based on the Lilienfeld's first transistor architecture [8]. The electrical characteristic of Bulk Planar Junctionless Transistor is given in paper [10]-[13]. The SOI Junctionless Transistor design is present in the paper [1] [14]-[19]. The Double Gate Junctionless Transistor analysis is presented in the paper [20]-[25] and the Tunnel Junctionless Transistor [26] [27]. The multigate transistor is explained in the paper [29]-[31], and gate all around in [32] [34]. Colinge et al. has successfully fabricated the junctionless nanowire transistor [1]. S. Gundapaneni et al. has demonstrated Bulk Planar Junctionless Transistor and SOI Junctionless transistor [10]. Ratul Kumar Baruah et al. has reported about analog performance of Bulk Planar Junctionless Transistor [13]. Chan-Hoon Park has done electrical characterization of Junctionless Transistor [37]. J. P. Duarte et al. has given bulk current model for long channel double gate Junctionless transistor [25]. A. Gnudi et al. has done analysis of threshold voltage variability due to random dopant fluctuations in Junctionless FETs [17]. Haijun Lou et al. has demonstrated Junctionless Nanowire Transistor with a Dual-Material Gate [35].

The paper is organized as follows. First the introduction and device concept is outlined. In section 2. Different types of junctionless transistor structure are explained and in section 3. Results and discussion are presented in

section. Finally, section 4 presents the conclusion of Bulk Planar Junctionless Transistor, SOI Junctionless Transistor, Double Gate Junctionless transistor and Bulk Junctionless Transistor.

II. Structures of junctionless Transistor

A. SOI Junctionless Transistor:

A BOX layer is formed on the bulk silicon layer, above it a thin device layer is deposited. Above device layer a thin gate dielectric layer is deposited and a metal layer which have a work function of 5.1 eV. The metal layer should have opposite work function with respect to the device layer. There is dielectric isolation at the bottom of the device layer. The device have uniform doping in channel, drain and source region. There is no conduction between the source and drain when zero bias is applied, the device layer is depleted of carrier due to workfunction difference. Conduction takes place when a positive bias is applied to the gate the thin device layer comes out of depletion. The typical parameters and device dimensions are device layer thickness is 10nm, donor doping concentration is taken to be $1.5 \times 10^{19} \text{ cm}^{-3}$, gate work function 5.1 eV and oxide thickness is of 1nm. To depict the physical behavior of the device the self-consistent drift-diffusion equations for electrons and holes need to be considered; for well-to-drain nonlocal tunneling, band-gap narrowing and Schottky–Read–Hall mechanisms were included. The mobility model includes both doping and transverse-field dependence.[10] The nonlocal BTBT model take into account tunneling along the lateral direction (i.e., tunneling of carriers between the source, channel, and drain regions) and in the vertical direction (i.e., tunneling of carriers between the n-type device layer and the substrate). Band-gap narrowing (BGN) due to high doping is modeled using Old Slotboom BGN model. The direct tunneling model for gate leakage calculations is turned OFF assuming high- κ metal gate stack. [12].

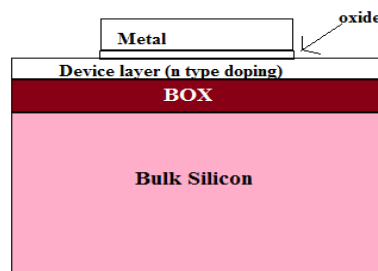


Fig.2 SOI Junctionless Transistor [10].

B. Bulk Planar Junctionless Transistor

In BPJLT the device layer is formed above the bulk silicon, bulk silicon and device layer have opposite polarity. There is a junction depth of X_j between the device layer and bulk silicon. The device do not have junction in vertical direction but there is junction in horizontal direction. Thin gate dielectric and metal is present above the device layer with workfunction of 5.1 eV .The gate should have opposite workfunction with respect to the device layer. There is no conduction between source and drain when zero bias is applied the device layer is depleted from top and bottom due to the work function difference between gate and device layer at top and due to opposite doping of device layer and bulk at bottom. Device layer will come out of depletion as we apply positive bias to the gate. The typical parameter and device dimensions for BPJLT are device layer 10nm, donor doping concentration is taken to be 1.5×10^{19} , gate work function 5.1 eV and oxide thickness is 1nm, BOX thickness 100nm. In order to depict the actual behavior of device several models and mechanisms need to be included such as self-consistent drift-diffusion equations for electrons and holes, models for well-to-drain nonlocal tunneling, band-gap narrowing and Schottky–Read–Hall mechanisms. The mobility model includes both doping and transverse-field dependence [10]. The nonlocal BTBT model take into account tunneling along the lateral direction and in the vertical direction. Band-gap narrowing (BGN) due to high doping is modeled using Old Slotboom BGN model [12].

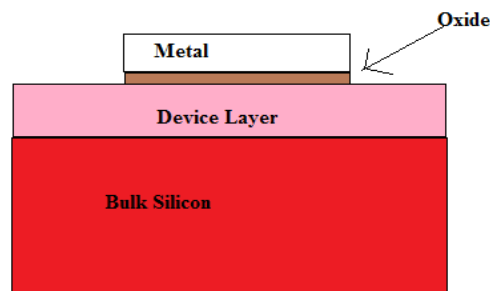


Fig 3 Bulk planar Junctionless transistor [10].

C. Double Gate Junctionless Transistor:

DGLT consist of two gate at top and bottom of device layer. The device layer is uniformly doped and gates are placed above and bottom of device layer having opposite workfunction with respect to the device layer. It has same doping in the source, drain and channel and gate, channel length can be considered equivalent to gate length. When the applied voltage is less than threshold voltage the channel will be depleted of carrier and there will be no conduction. As we apply voltage more than threshold voltage to gate, channel will come out of depletion and start conduction. When the applied voltage is equal to the flat band voltage then bulk conduction takes place and if we further increase the voltage then there will be a surface current flowing in the device. The typical device parameter are channel doping $1.5 \times 10^{19} \text{ cm}^{-3}$, Gate workfunction 5.3 eV, Gate oxide (SiO_2) thickness 1nm, Physical gate length 20-100nm, Body thickness 10nm. L_G and L_S as shown in Fig. 4 are the length of source and drain respectively. For the accurate simulation of this device, models considered are the Fermi-Dirac model without impact ionization, doping concentration-dependent carrier mobility and electric field-dependent carrier model. Band gap narrowing model was included. Shockley-Read-Hall (SRH) recombination generation were included to account for leakage currents [20]. To study in detail the electrical properties of short-channel devices quantum corrected 2D full band Monte Carlo simulator are used [21].

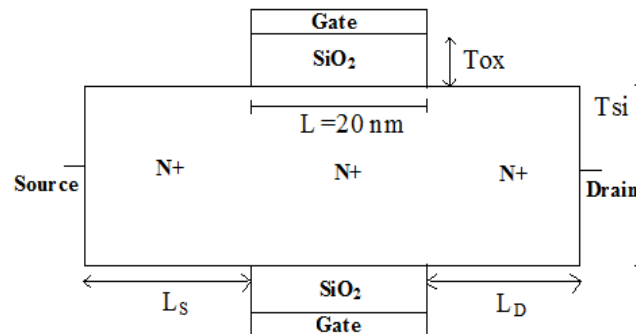


Fig 4 Double gate Junctionless Transistor [20]

D. Tunnel Junctionless Transistor:

It consist of a uniformly doped device layer with two isolated gate of different workfunction material to obtain the tunnel FET behavior. It have same doping concentration in source, drain and channel region. This structure has the advantage of both the Junctionless transistor and tunnel FET. The Si layer is heavily doped with two isolated gate P-Gate and control Gate for better controllability of the device. The isolated gate with different workfunction material are used to make the device layer below it intrinsic and p type so that it forms N^+-I-P^+ device structure from $N^+-N^+-N^+$. For zero bias condition the barrier between N and P layer will more and there will less probability of tunneling and there will no conduction of current. Application of positive bias to control gate the barrier between the N and P layer will decrease and there will be tunneling and conduction takes place. The device parameter taken for simulation are silicon film thickness of 5nm, gate oxide thickness 2-nm, workfunction for control gate 4.3 eV, work function for P-gate 5.93 eV, high-k dielectric (Si_3N_4) $k = 7.5$, low-k spacer (SiO_2) $k = 3.9$. In order to simulate this device, nonlocal band-to-band tunneling (BTBT) [17] model is required. The nonlocal BTBT model takes into account a tunneling along the lateral direction. This model also include the mobility effect. Band-gap narrowing (BGN) model is also enabled due to high doping concentration in the channel. Shockley-Read-Hall (SRH) recombination model is also included because of a presence of high impurity atom in the channel and also consideration of an interface trap (or defect) effect, the effect of Fermi Dirac statistics in the calculation of the intrinsic carrier concentration[26]. The quantum confinement effect and interface trap effect on BTBT in TFETs are also enabled, by inclusion of quantum confinement (QC) model given by Hansch, and trap-assisted tunneling (TAT) model. The gate leakage current model is not included, with the assumption of high-k metal gate stack [26].

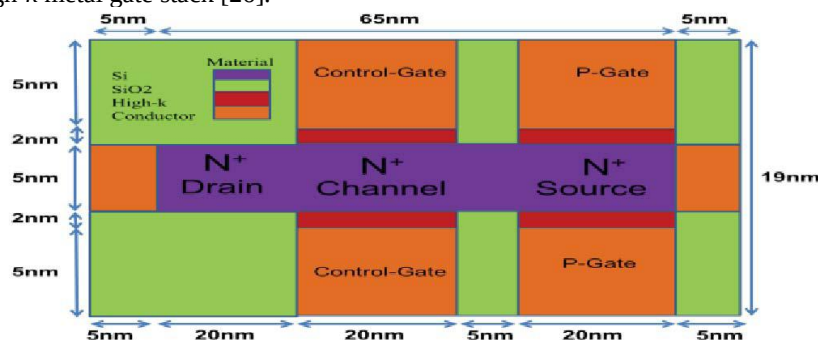


Fig. 5 Tunnel Junction less Transistor [26].

III. Discussion

The mobility of junctionless transistor is reduced due to high channel doping but the small on state surface field increases the mobility of the device. Junctionless transistor have better DIBL and subthreshold slope than inversion mode devices. Junctionless transistor have DIBL of 48 mV/V, subthreshold slope of 66.2 mV/decade, I_{ON} 1000 $\mu A/\mu m$ and I_{ON}/I_{OFF} ratio of 5×10^6 compared to Inversion mode transistor having DIBL 153 mV and subthreshold slope 83.8 mV/dec has I_{ON} 1000 $\mu A/\mu m$ and I_{ON}/I_{OFF} ratio of 5×10^6 already been reported [7]. For bulk planer and SOI junctionless transistor the I_{ON} is reported to be around 10^{-3} $\mu A/\mu m$ and I_{ON}/I_{OFF} ratio around 10^5 [10]. The I_{ON}/I_{OFF} , DIBL, subthreshold slope of Bulk planer junctionless transistor is better than SOI junctionless transistor for same device dimensions. The Bulk planer have better device characteristic than SOI due to junction isolation at the bottom, there is better depletion of carrier junction. BPJLT is found to have better drain current, transconductance, output conductance, output resistance, early voltage, intrinsic gain, unity gain frequency as compared to SOIJLT [20]. For double gate threshold voltage is reported to be 0.4 V for thickness of 5nm and DIBL of 40 mv [21]. $I_{ON} = 52.3$ A/ μm for independent double gate junctionless transistor has already been reported. The double gate junctionless transistor exhibit better device characteristic than conventional Double gate FET. It has been reported an I_{ON}/I_{OFF} of 6×10^8 and subthreshold slope of 38 mv/decade in case of Tunnel junctionless transistor. The ON current and OFF current for tunnel junctionless transistor are reported to be ~ 36 $\mu A/\mu m$ and $\sim 5 \times 10^{-14}$ A/ μm respectively [26].

IV. Conclusion:

A review study of different types of Junctionless transistor is presented in paper. The bulk planar Junctionless transistor have better device characteristic than SOI junctionless transistor. The bulk planar Junctionless transistor exhibits better control on channel due to junction isolation and can be varied by well bias and well doping. Double gate junctionless transistor has two gate for better controllability of the channel. Tunnel junctionless transistor have two gate to obtain the properties of tunnel FET. The junctionless transistor advantage can be exploit by taking the very thin silicon channel. The junctionless transistor need more reliability and variability study. The junctionless transistor can also be implemented using strained silicon. As the device dimensions are reducing to nano level the reliability and variability issues are of big concern and needs focus of researchers.

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