



## DESIGN OF EFFICIENT CLOCK GATED DET-FLIPFLOP FOR ASYNCHRONOUS DATA SAMPLING

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**Abstract:** Energy consumption has become one of the important factors in digital systems. Storage elements and the clock distribution of an IC consumes large power in case of Synchronous design. Energy efficiency which plays the critical role in low power circuit design is improved by using double edge-triggered flip-flops (DETFFs), since they can maintain the same throughput as single edge-triggered flip-flops (SETFFs) while only using half of the clock frequency. Clock gating is another known technique to reduce the dynamic power of idle cycles. An asynchronous data sampling is introduced at the output side by incorporating clock gating with DETFFs to further reduce dynamic power consumption, it causes data miscommunication error between clock edge. Three special clock-gating strategies are used to mitigate this issue in DETFFs and the parameters such as power, area are evaluated and compared. The proposed circuit was simulated in MICROWIND and MODELSIM 6.3f. The proposed approach demonstrates that the dynamic power reduced considerably and the simulation results indicated that the proposed circuit is capable of significant delay and power saving.

**Keywords:** asynchronous data sampling, dynamic power consumption, DETFF, clock gating

### I Introduction

Power consumption of very large scale integrated VLSI chips is growing to be an increasingly crucial problem as chip densities increase. Therefore the improvement of such circuits such as a decrease in power consumption, without weakening other characteristics, is very important in VLSI industry. For a sequential system, the power spent on the clock-tree or the timing components is a major source of all the power consumption.

The clock system, which consists of the clock distribution network and timing elements (flip-flops and latches), is the major power consuming components in a VLSI system. It accounts for 30% to 60% of the total power dissipation. As a result, deducing the power consumed by flip-flops will have a deep impact on the total power consumed. In modern integrated circuits (ICs) the power consumed by two ways. One effective and efficient approach[1] is Double edge triggered flip flop (DETFF). Dual edge clocking requires Dual Edge-Triggered Storage Elements (DETSE), capable of capturing data on both rising and falling edge of the clock. Main advantage of DETSE is their operation at half the frequency of the conventional single-edge clocking, while obtaining the same data throughput. The second technique is Clock-gating for a large digital system, clock-gating technique is used to reduce the power consumed on idle circuitry in the design. The DETFF and clock gating combined together [2] to further reduce dynamic power but it introduces the asynchronous data sampling problem between the clock edges at the output side it creates the data miss-communication error. This paper deals with various clock gated DETFF proposed to analyze the sampling problem and three approaches are designed to filter out this problem and the parameters are compared.

### II Asynchronous Data Sampling

The clock gated system has the terminology as global clock **CLK**; the (internal) gated clock signal **C**;, clock-gating control signal **CG**; , input data **D**; and , output data **Q**. the internal clock controls the gated circuits. The internal clock is separated from the global clock. If the internal clock is not synchronized with the global clock when the gating signal is in non-active state, then the internal clock needs to switch immediately to match the global clock. This switching is extra and not synchronized with the external clock, which creates an asynchronous data sampling, which is shown by the output changing between clock edges. Each clock-gating transition has the potential to create the asynchronous sampling issue. The specific conditions deals with the creation of asynchronous data sampling with different types of clock gated double edge triggered flipflop.

Figure.1 General block diagram of clock gated DETFF

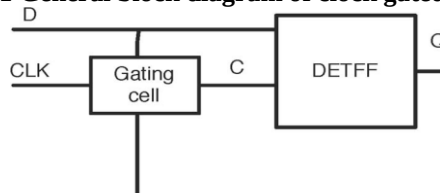


**Table.1 Conditions for asynchronous data sampling**

| Designs  | Conditions for asynchronous data sampling |
|----------|-------------------------------------------|
| GDETFF   | D changes when CLK#C                      |
| DETSRSFF | D changes when CLK=0(before rising edge)  |
| DHSCGFF  | D changes when CLK=0(before rising edge)  |

**A. Asynchronous Sampling in the Gated Double Edge-Triggered Flip-Flop With Transmission Gate(G\_DETFF)**

The G\_DETFF contains two major parts, the T\_DETFF[8] and the clock-gating circuitry which includes a comparator and the clock-gating module. The data signal arrives into the T\_DETFF and the comparator simultaneously, and the comparator checks the current data input D and the output Q. If D and Q are not equal, which means the input has changed since the last comparison, then an active gated clock signal will be generated. The gated clock signal will be sent to the T\_DETFF to trigger the storage signal. Then the input data signal will be passed to the output. Otherwise, the entire system remains in the previous state.

There are two variable factors when the flip-flop operates: which edge triggered the flip-flop for the last transition before clock gating was applied and 2) what is the value of **CLK** when clock-gating is deasserted. If the value of C does not equal the **CLK** when the circuit deactivates the clock-gating function, then the asynchronous sampling issue appears for the G-DETFF.

**B. Asynchronous Sampling in Low-Power Dual-Edge Triggered State Retention Scan Flip-Flop (DET SRSFF)**

The scan-retention mechanism is based on a prior art low-power overhead level-sensitive scan mechanism. The detsrff is composed of a pulse generator and a scan able static latch that has LFB (leakage feedback) to reduce leakage current. The new flip-flop with retention uses the scan latch as a low-leakage storage for retaining data during the power-down mode, and provides an extra path for restoring the data from the retention latch to the main flip-flop. The retention latch is built of low-leakage devices, such as high threshold transistors, with the back bias capability. If gate leakage is an issue, transistors in the retention latch can be implemented as thick gate oxide devices.

Particularly for DET SRSFF, the asynchronous data transition occurs when an input change while **CLK** equals 0. Because the input changed, the gating signal is deasserted, so Node connects with **CLK** again. Then the value of Node changes from 0 to 1 immediately. The result is an unwanted pulse that triggers the flip-flop between clock edges where that output data signal should be held and is observed at before rising edge.

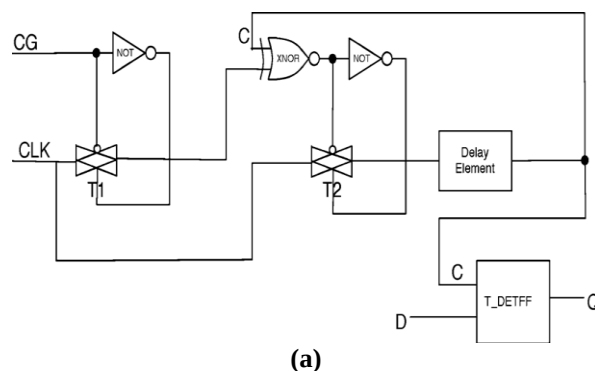
**C. Asynchronous Data Sampling in the Double Edge-Triggered Half-Static Clock-Gated D-Type Flip-Flop (DHSCGFF)**

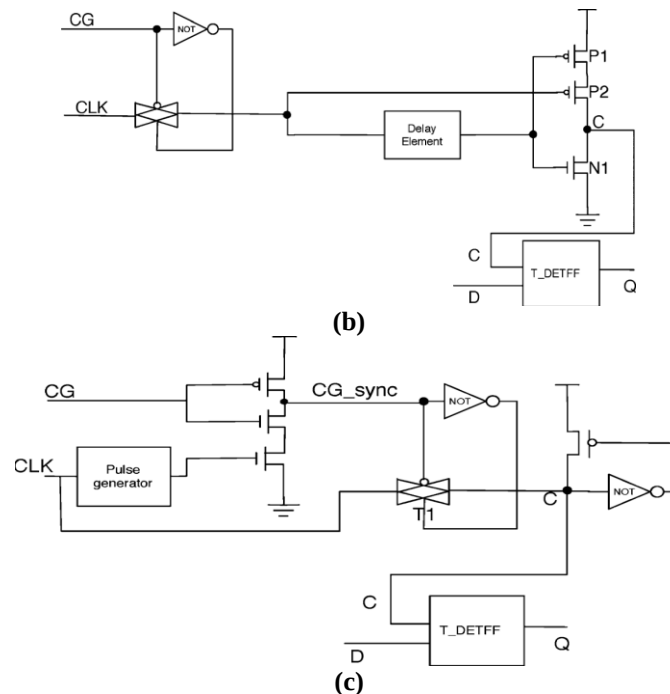
The gated clock signal **R** stays 0 when gated (inactive). So if the input data changed when **CLK** =0[7] , then the value of **C** will change to 1 immediately, and  $\overline{C}$  will follow as the complement of C. An asynchronous clock edge of C triggers the flip-flop, causing the asynchronous data sampling. After each data transition, the gated signal C goes back to 0 and stays low until the next transition.

**III Technique used to Avoid Sampling Problem**

This section describes how the sampling problem addressed and removed. Generally Sampling problem shares the same root cause, namely the discontinuity between the global and internal clock. If the internal clock differs from the global clock when clock gating is discontinued, then the internal clock event is transmitted immediately. There are three different methods used to overcome asynchronous data sampling. In figure.2(a) describes comparator prevents the asynchronous sampling occurs in this implementation

**Figure 2: The Different Methods Used To Avoid Asynchronous Data Sampling Problem**





Asynchronous sampling occurs when D changes at the moment that **CLK** differs from 0. During the comparison of CLK and c the switch T2 is in off state at the condition CLK# C. In the next half cycle the C will be allowed to synchronize with CLK when T2 is in ON condition.

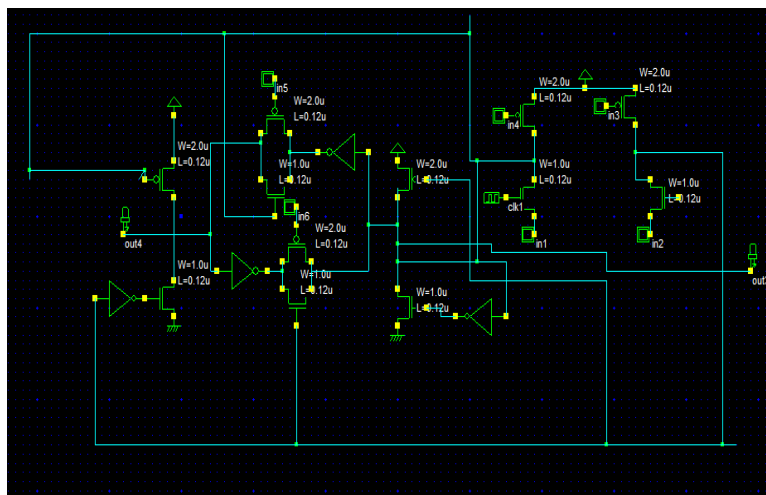
The figure.2(b) explains C normally stays at 0. When D changes while the **CLK** is 1, transistor P2, the one closer to **CLK**, will be turned OFF immediately, and will remain the same. When **CLK** goes back to 0 (i.e., a falling edge), P2 is ON, and because of the delay element, P1 will stay ON for the time needed to trigger the flip-flop.

The figure.2(c) The pulse generator detects and generates a positive pulse for every edge of the **CLK**. No matter when D changes, even though the comparator's result is ready immediately, the ON signal of transmission gate T1 only generates at clock edges. So C and **CLK** are synchronized, and the asynchronous sampling is avoided in this design.

#### D. Clock Gated Sense Amplifier Dual Edge Triggered Flip Flop

The sensing stage is the same as DET-SAFF. Since the generated PULS signal is more heavily loaded than that of DET-SAFF, a modified Nikolic's latch [9] is used. It does not require any clock signal and provides the most stable operation. The inner holding topology is modified in order to attain buffered differential outputs, Q1 and QB1, with minimized load capacitances. In the clocking stage, Q1 and QB1 are used to generate X and Y instead of using Q and QB. This helps to improve the performance of CG-SAFF significantly.

**Figure 3: The new clock gated sense amplifier dual edge triggered flip flop: (sensing and latching stage)**



In order to eliminate the redundant transitions in the pulse generator, the CG-SAFF is constructed. It utilizes the DETSAFF design as a baseline and incorporates the clock gating technique. In CG-SAFF, the clock gating

technique is implemented by embedding a control circuit in the explicit pulse generator so that the PULS signal generation is disabled in a redundant event.

#### IV RESULTS AND DISCUSSIONS

**Figure 4.(a) Proposed G-DETF without sampling problem**

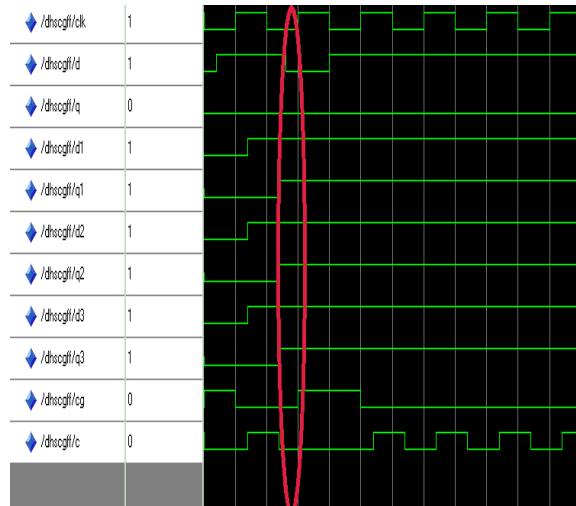
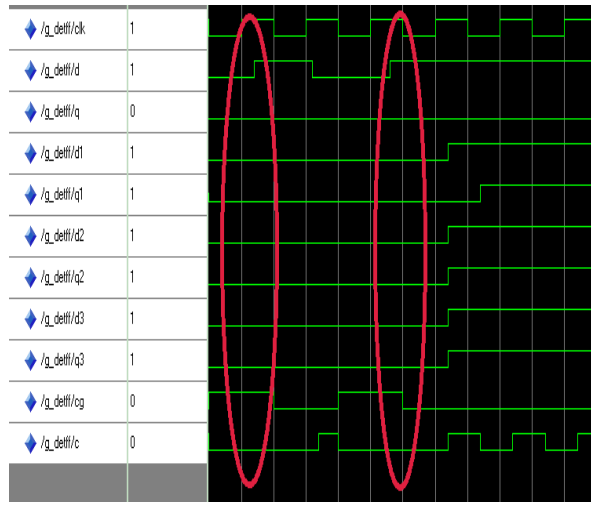


**Figure 4.(b) Proposed DHSCFF without sampling problem**



The asynchronous data sampling is eliminated between the clock edges at which the condition of clk#0 and clk=0(before rising edge)

**Table 2: Parameter analysis of different proposed flipflops**

| Type      | Power (mw) | Area(gate count) | Delay( $\mu$ s) |
|-----------|------------|------------------|-----------------|
| G-DETF    | 117        | 56               | 13.53           |
| DHSCGFF   | 119        | 51               | 13.69           |
| DET-SRSFF | 117        | 64               | 14.508          |
| DETSAFF   | 90         | 25               | 6.824           |

The above table describes the analysis of different proposed flipflop after the asynchronous data sampling problem removed. The power consumption of DETSAFF is comparatively less as 90(mw) than the other flipflop same as the area occupied by the flipflop (gate count) as 25 the over all delay is 6.824  $\mu$ s also reduced. Therefore the DETSA flipflop is produced effective result without asynchronous data sampling is analyzed from the table.

#### V Conclusion and Future Enhancement

Because of the high demand of mobile devices on power efficiency, a variety of power reduction techniques emerged for optimization and improvement. Various modules of low power circuits has been proposed and designed, based on the dual edge triggered structure. To reduce the dynamic power consumption, a number of low-power techniques such as clock gated is implemented at the system level and low-power circuit design methodologies have been proposed and adopted. DETFF achieves substantial power reduction by incorporating dual edge triggering and clock gating. However, when applying clock gating into a DETFF, a data transition error may appear at the output between clock edges due to asynchronous data sampling. The asynchronous data sampling has been eliminated by three special clock gating techniques. In this project, several solutions have been provided to avoid the asynchronous sampling problem in clock-gated DETFF and the different clocking strategies are analyzed and the parameters like power and area are compared.

#### VI References

- [1]. A. G. M. Strollo, E. Napoli, and D. De Caro, 2003 June "New clock-gating techniques for low power flip-flops," in Proc. Int. Symp Low Power Electronics and Design.
- [2]. C.-C. Yu, 2008, "Low-power double edge-triggered flip-flop circuit design," in Proc. Int. Conf. Innovative Computing Information and Control, pp. 114–119.
- [3]. H. Karimiyan, S. M. Sayedi, and H. Saidi, 2010 "Low-power dual-edge triggered state retention scan flip-flop," IET Comput. & Dig. Techniques, vol. 4, no. 5, pp. 410 ,419,.
- [4]. N. Nedovic and V. G. Oklobdzija, Oct. 2005 "Dual-edge triggered storage elements and clocking strategy for low-power systems," IEEE Trans. Very Large Scale Integration (VLSI) Syst., vol. 13, no. 5, pp. 577–590,.
- [5]. P. Zhao, J. McNeely, P. Golconda, M. A. Bayoumi, R. A. Barcanas, and W. K.W Kuang, Jun. 2007 "Low-power clock branch sharing double-edge triggered flip- flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 3.
- [6]. Q. Wu, M. Pedram, and X. Wu, Mar. 2000 "Clock-gating and its application to low power design of sequential circuits," IEEE Trans. Circuits Syst. I: Fundam.Theory Appl vol. 47, no. 3, pp. 415–420,.

- [7]. W.-S. Tam, S.-L. Siu, C.-W. Kok, and H. Wong, 2010, "Double edge-triggered half- static clock-gated D-type flip-flop," in Proc. IEEE Int. Conf. Electron Devices Solid- State Circuits (EDSSC), pp. 1–4.
- [8]. X. Wang and W. H. Robinson, 2010 "A low-power double edge-triggered flip-flop with transmission gates and clock gating," in Proc. IEEE Int. Midwest Circuits and Systems (MWSCAS), pp. 205–208.
- [9]. Myint Wai "Phyupower-Efficient Explicit-Pulsed Dual-Edge Triggered Sense-Amplifier Flip-Flops " Ieee Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 19, No. 1, 2011

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