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EFFICIENT LOCALIZATION SCHEME FOR A LOW POWER CONTENT ADDRESSABLE MEMORY BASED ON XNOR CELL

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Abstract- In recent developments in the design of large-capacity content-Addressable memory. A CAM is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuit. CAMs are particularly popular in network routers for packet forwarding and packet categorization but they are also beneficial in a variety of other applications that require high-speed table lookup. The main CAM-design has required on reducing power consumption associated with the large amount of parallel active circuit, without change in speed or memory density. . In CAM-design techniques at the circuit level and at the architectural level. At the architectural level we review three methods for reducing power consumption and area.

Keywords: content addressable memory, pre computation, parity bit method, match line, XNOR CAM

I INTRODUCTION

Content-addressable memory (CAM) is a special type of computer memory used in certain very high speed searching applications. It is also called as associative memory, associative storage or array. Binary CAM is the simplest type of CAM which uses data search words consisting entirely of 1s and 0s. Ternary CAM (TCAM) allows a third matching state of "X" or "Don't Care" for one or more bits in the stored data word, thus adding flexibility to the search. Content-addressable memory is regularly used in computer networking devices. (eg) when a network switch receives a data frame from any one of its ports, and update their internal table with the frame's source MAC address and the port it was received on. It then looks up the target MAC address in the table to determine what port the frame needs to be forward to, and sends it out on that port. The MAC address table is generally implemented with a binary CAM so the destination port can be found quickly, reducing the switch's latency.

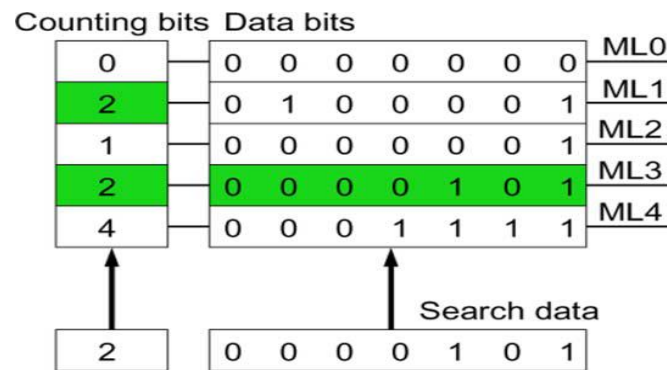
II CONTENT ADRESSABLE MEMORY

Content-addressable memory is a special type of computer Memory used in certain very high speed searching application. It is also known as associative memory, associative array. In a traditional memory input is the address of the memory location that we are interested and output will be the content of that address. CAM is the reverse and a content-addressable memory is a critical device used for applications involving asynchronous transfer mode (ATM), communication networks, LAN bridges, databases, lookup tables, and tag directory, due to its high-speed data search capability [1]. A CAM is a functional memory which have a large amount of stored data that simultaneously compares the input search data with the stored data. The huge number of comparison operations required by CAMs consumes a large amount of power.

A. Pre computation method

This concept pre-compare several bits of the match line in advance. Throughout the mechanism of the pre-comparison scheme, it can decide that whether the other bits would be compared or not. If the pre-comparison bits are match, the other bits must be compared in the different step. And also if the pre-comparison bits are mismatch, then the remaining bits will not be compared. Pre-comparison circuit is between the match line circuits and pre-charged circuits. Discharging path from the pre-charged circuit to the match line circuit will be disconnected only when any one bit in the pre-comparison circuit is mismatch to turn off the discharging path. On the other hand, the pre-comparison circuit will send a control signal from the comparison result to the output logic circuit for deciding the output value. The previously mentioned pre-computation and all other existing designs shares their common property. The ML sense amplifiers essentially has to distinguish between the matched ML and the 1-mismatch ML. This makes CAM designs faster or latter face challenges since the driving strength of the single turned-on path is getting weaker after each process generation while the leakage is getting stronger. This problem is usually referred to as I_{ON}/I_{OFF} . We propose a new supplementary bit that can concurrently boost the sensing speed of the ML and at the same time improve the I_{ON}/I_{OFF} of the CAM by two times. Figure 1 shows data searching method of pre computation.

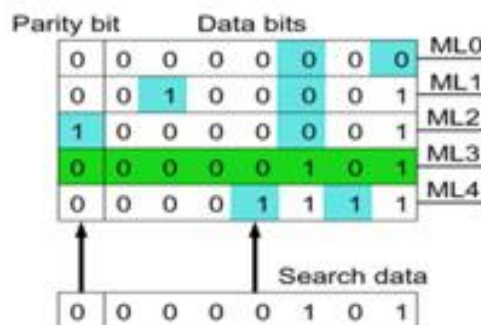
Figure 1 search method using pre computation



B. parity bit method

This method is same as that of pre computation method, the data segment of parity method extra one bit is derived from original data that indicate whether the data is even or odd number of “1”s is shown in figure 2. The obtained parity bit is placed directly in word and ML. Thus the new design has the same interface as the conventional CAM with one extra bit is added. During the search operation, there is only one single stage as in CAM. Hence, this parity bits does not improve the power consumption[4]. Though, this additional parity bit, reduces the sensing delay and boosts the driving strength of the 1-mismatch case (which is the worst case) by half.

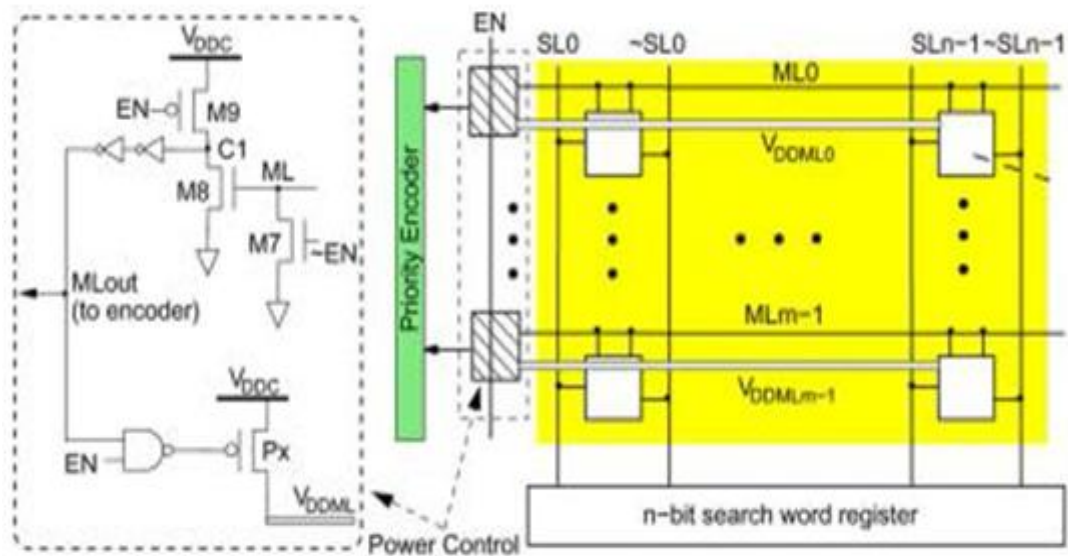
Figure 2 search method using parity method



C. Gated power match line sense amplifier

The CAM architecture is shown in figure 3. The CAM cells are organized into word and columns (bit). Each cell has the same number of transistors as the rows conventional P-type NOR CAM and use a similar ML structure. However, the “COMPARATOR” unit, transistors M1-M4, and the “SRAM” unit, i.e., the cross coupled inverters, are powered by two separate power rails, namely VDDML and the VDD, respectively. The VDDML is independently controlled by a power transistor (Px) and a feedback loop that can auto turn-off the ML current to save power. The purpose of having two separate metal rails of (VDD and VDDML) is to completely isolate the SRAM cell from any possibility of power disturbances during “COMPARE” cycle. The gated-power transistor Px, is controlled by a loop, that is denoted as “Power Control” which will automatically turn off Px once the voltage on the ML reaches a certain threshold value[4]. At the beginning of each cycle, the ML is first initialized by a control signal EN. At this time, signal EN is set to low and the power transistor Px is turned OFF. This will make the signal ML and C1 initialized to ground and VDD, respectively. After that, the signal EN turns HIGH and initiates the COMPARE operation. If one or more mismatches happen in the CAM cells, the ML will be charged up. All the cells of a row will share the limited current offered by the transistor Px, despite whatever number of mismatches. When the voltage of the ML reaches the threshold voltage of transistor M8 (i.e., Vth8), voltage at node C1 will be pulled down. But very minor delay, the NAND2 gate will be toggled and thus the Px is turned off again. The ML is not fully charged to VDD, but limited to some voltage to some extent above the threshold voltage of M8 (Vth8).

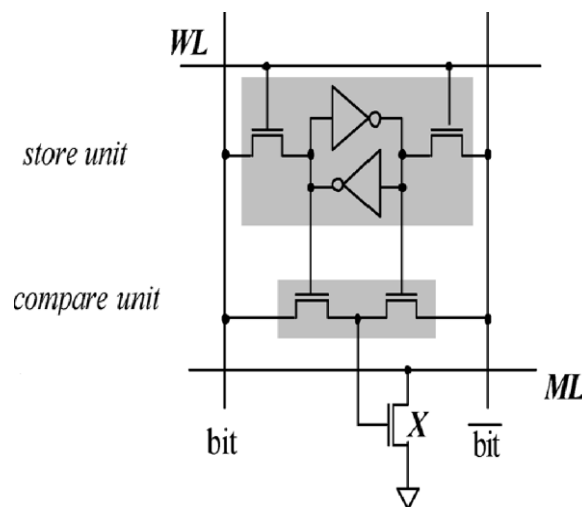
Figure 3 schematic of CAM



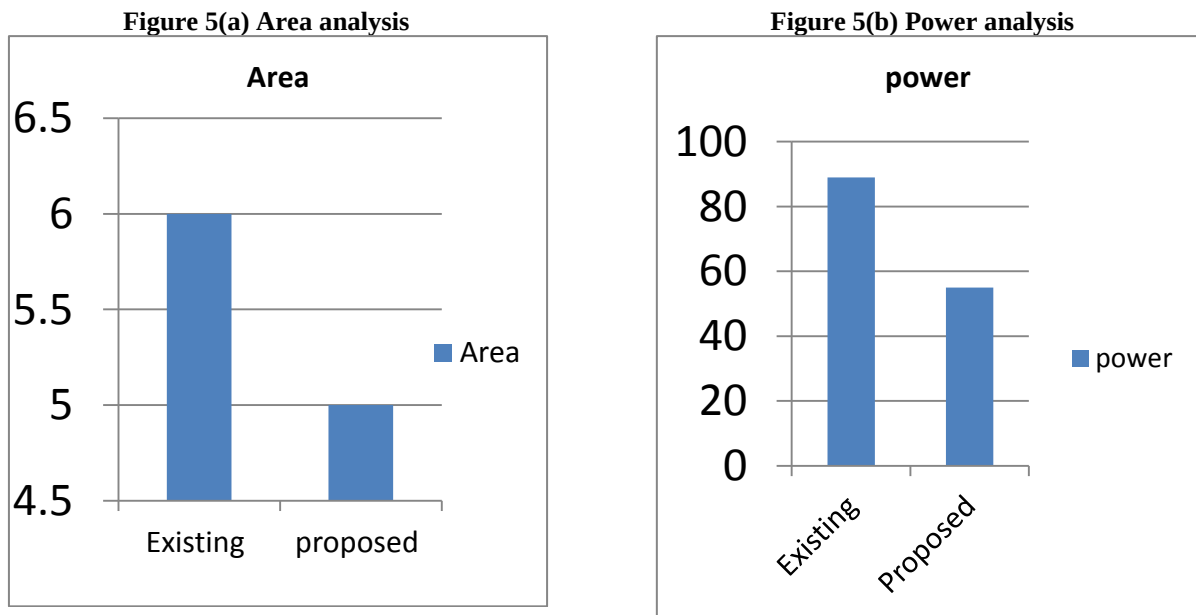
III PROPOSED XNOR CAM CELL

Traditionally, there are two types of CAM designs. One is NOR-type and the other is NAND-type. In NOR-type CAM design, the CAM cell is usually XOR-type, and the pull-down transistors of each CAM cell are ordered in NOR type. During precharge phase, the match line is initially precharged to high. If one or more cells are mismatched in a CAM, the match line would be discharged. Only when all cells are matched, i.e., the search data are identical to the stored data, the match line can retain logic high as in the precharge phase. Because the pull-down path is very short, in case of a mismatch the match line is discharged to low value quickly. Thus, the NOR-type CAM provides the best search performance. Note that the pull-down transistors in NOR type is beneficial for search performance, but they contribute a lot of drain capacitances to the match line. This results in more power dissipation in match line switching. Because in many applications most of the CAM words are mismatched, a large number of match line switches would consume a significant dynamic power. For example, the CAM used in the TLB or cache memory, matching of at most one word on each lookup, implies that almost all the match lines would be discharged to low value, and then be charged to high before the next search. Consequently, the NOR-type CAM is power inefficient, even though it can provide the best performance[2]. XNOR type CAM cell is shown in figure 4.

Figure 4 XNOR CAM cell



IV PERFORMANCE ANALYSIS



Area and Power analysis for conventional CAM cell and XNOR CAM Cell has been calculated that is shown in figure 5(a) & 5(b). From this clear that we obtained Area and Power has been minimized in proposed method.

V SIMULATION ANALYSIS

Figure 6 Layout of CAM cell

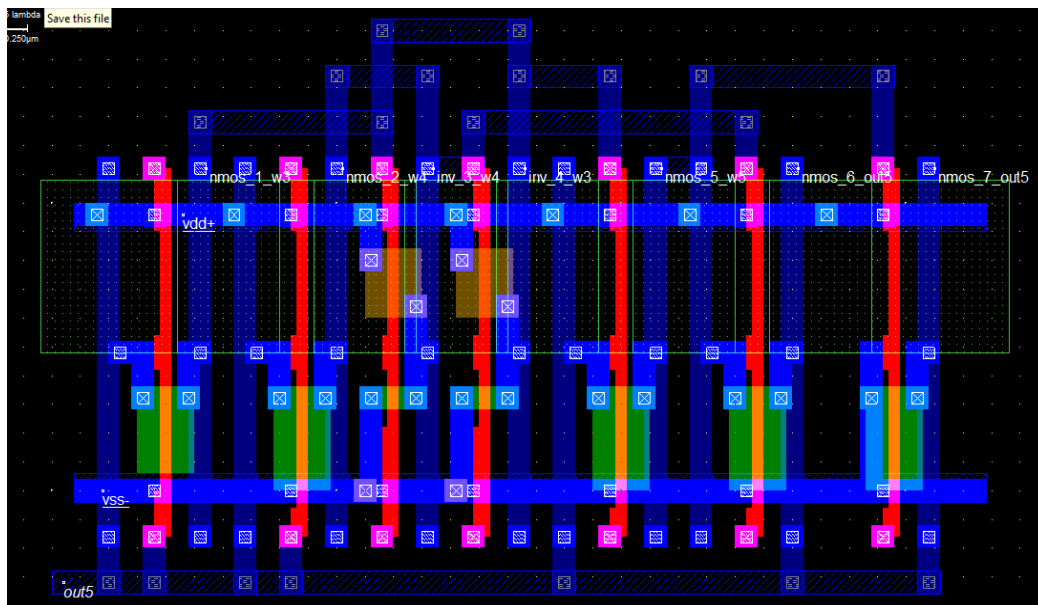


Figure 6 explains proposed CAM cell schematic diagram. Figure 3.9 shows layout of CAM cell layout using XNOR Cell. Area of the XNOR CAM Cell occupied 5T space. This architecture shows good results in terms of area and dynamic power consumption.

Figure 7 Simulation of XNOR CAM Cell

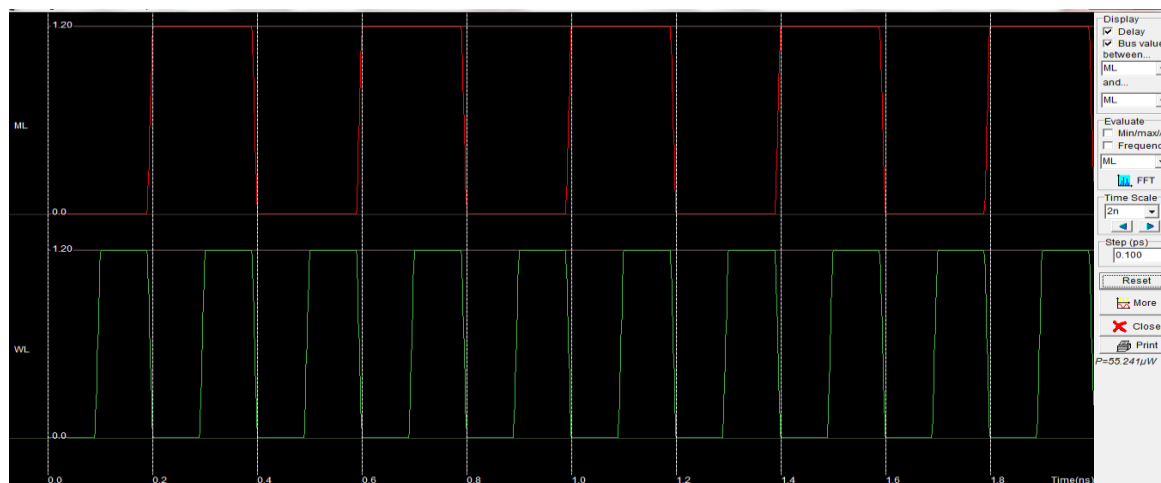


Figure 7 reveals proposed CAM cell power consumption WL and ML. out1 denotes select line. it consume 55.24 μ W power used by single CAM cell. In proposed CAM cell power consumption is reduced.

VI CONCLUSION

In effective gated-power technique and a parity-bit based architecture that offer several major advantages, namely reduced peak current, average power consumption, boosted search speed and improved process variation tolerance. It is more stable than recent designs while maintain their low-power consumption property. When compared to the existing CAM cell power has been reduced from 89.83 μ W to 55.24 μ W. Area also reduced to 5T in XNOR type proposed CAM cell. According to our simulations its area overhead is about 11%. It is therefore the most suitable design for implementing high capacity parallel CAM in sub-65-nm CMOS technologies. This discussion is extended to these cells which are used to design a match line of CAM mainly the power consumption of CAM due to match line sensing techniques and search line driving approaches which are used to reduce the power consumption of CAM. In future many techniques can be used to design Low power CAM.

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