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Design & Implementation of High Speed N- Bit Reconfigurable Multiplier Using Vedic Mathematics for DSP Applications

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Abstract: This paper proposed to design & implement high speed N-bit multiplier using vedic mathematics for DSP Application. The term “veda” means “knowledge”. The Veda are divided into four main section the Sama-veda Rig-veda, Yajur-veda and the Atharva-veda. The vedic mathematics deals with the fourth section i.e atharva_ veda. The vedic mathematics based on sixteen principal known as sixteen sutra. It was rediscovered by Sri Bharati Krishna Tirthaji. From Vedas between 1911 and 1918. The simplicity of Vedic Mathematics means that calculations can be carried out mentally. Digital signal processing deals with the fast processing , by using vedic mathematics we can design high speed N-bit multiplier which is used for DSP application.

I. Introduction

Digital signal processing (DSP) is the mathematical manipulation of an information signal to modify or improve it in some way. DSP is used to represent discrete time, frequency & various discrete domain signals by a sequence of numbers or symbols and the processing of these signals. Digital multipliers are indispensable in the hardware implementation of many important functions such as Fast Fourier Transforms (FFTs) and Multiply Accumulator (MAC). Speed of the digital signal processor is largely determined by the speed of the multiplier. Since, processor spend considerable amount of time in multiplication, hence speed of processor can be improved by a faster multiplier. Multiplication can be implemented using many algorithm such as array algorithm, booth algorithm. In array multiplier In array multiplier, multiplication is carried out by using add & shift method. The method is slow, however, as it involves many intermediate additions. The computation time to perform an additions operation takes a lot of time. In booth's algorithm, it effectively skips over runs 1s & runs of 0s that it encounters in multiplier. This skipping reduces the average number of add – subtract steps & allow faster multiplier to be designed, although at the expense of more complex timing & control circuitry. As compared to above method, vedic multiplier is more efficient than the conventional multiplier .This paper presents a simple digital multiplier architecture based on the ancient Vedic mathematics Sutra (formula) called Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra which was traditionally used for decimal system in ancient India.

II. Multiplication algorithm

There are sixteen principles of vedic mathematics. These sutra performs various operations such as arithmetic, algebraic & geometric. They are listed as follows.

- 1) Ekadhikena Purvena: The Sutra means: “By one more than the previous one
- 2) Nikhilam Navatashcaramam Dashatah: The formula: “all from 9 and the last from 10”
- 3) Urdhva-Tiryagbyham: Vertically and crosswise
- 4) Paraavartya Yojayet: This performs the operation “Transpose and adjusts”.
- 5) Anurupye Shunyamanyat: In this, If one is in ratio, the other is zero.
- 6) Shunyam Saamyasamuccaye: In this, it performs operation,” When the sum is the same that sum is zero”.
- 7) Puranapuranyam: It means “By the completion or non-completion”.
- 8) Chalana-Kalanabyham: Differences and Similarities
- 9) Yaavadunam : Whatever the extent of its deficiency
- 10) Vyashtisamanstih: Part and Whole
- 11) Sankalana-vyavakalanabhyam : By addition and by subtraction
- 12) Shesanyakena Charamena: It Performs “The remainders by the last digit”.
- 13) Sopaantyadvayamantyam: This type of sutra follows “The ultimate and twice the penultimate”
- 14) Ekanyunena Purvena: In this, it performs “By one less than the previous one”

15) Gunitasamuchyah: In this, The product of the sum is equal to the sum of the product.

16) Gunakasamuchyah: This type of sutra follows “The factors of the sum is equal to the sum of the factors”.

All the above vedic mathematics principal perform various operation. In our paper, we are working on principle urdhva tiryagbham.

III. Steps involved for multiplication using vedic mathematics

The following is the example of vedic multiplier for three digit numbers. Both vertical & crosswise multiplications are showed below. The two digit multiplication example of 54 X 48 is given below

Step 1:

$$\begin{array}{r} 5 \quad 4 \\ \times 4 \quad 8 \\ \hline \end{array}$$

2

carry=3

Step 2:

$$\begin{array}{r} 5 \quad 4 \\ \times 4 \quad 8 \\ \hline \end{array}$$

9 2

Prev Carry =3 New Carry=5

$$\begin{array}{r} 40 \\ + 16 \\ \hline 56 \end{array}$$

Step 3:

$$\begin{array}{r} 5 \quad 4 \\ \times 4 \quad 8 \\ \hline \end{array}$$

2 5 9 2

Prev Carry=5

$$\begin{array}{r} 20 \\ + 25 \\ \hline \end{array}$$

The multiplication of 54 * 48 results 2592.

In the above example, the first step is to multiply, the LSB of multiplicand with LSB of multiplier. If the carry is generated then add carry with next result of cross multipliers. If carry is not generated then write the answer of product as a result. The product is carried out crosswise & vertically as it is shown in figure. The line diagram for four bit multiplication is given as follows

Step1	Step2	Step3	Step4	Step5	Step6	Step7
$\begin{array}{r} 1101 \\ \times 1010 \\ \hline \end{array}$	$\begin{array}{r} 1101 \\ \times 1010 \\ \hline \end{array}$	$\begin{array}{r} 1101 \\ \times 1010 \\ \hline \end{array}$	$\begin{array}{r} 1101 \\ \times 1010 \\ \hline \end{array}$	$\begin{array}{r} 1101 \\ \times 1010 \\ \hline \end{array}$	$\begin{array}{r} 1101 \\ \times 1010 \\ \hline \end{array}$	$\begin{array}{r} 1101 \\ \times 1010 \\ \hline \end{array}$

IV. Hardware Architecture

The design starts first with Multiplier design that is 4x4 bit multiplier. Here, “Urdhva Tiryakbhyam Sutra” or “Vertically and Crosswise Algorithm” for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is quite different from the traditional method of multiplication that is to add and shift the partial products. This Sutra shows how to handle multiplication of a larger number (N x N, of N bits each) by breaking it into smaller numbers of size (N/2 = n, say) and these smaller numbers can again be broken into smaller numbers (n/2 each) till we reach multiplicand size of (4 x 4). Thus, simplifying the whole multiplication process. For Multiplier, first the basic blocks that are the 4x4 bit multipliers have been made and then, using these blocks, 8x8 block has been made. The main advantage of the vedic multiplication algorithm (Urdhva-Tiryak Sutra) stems from the fact that it can be easily realized on hardware. The RTL view of 4-bit multiplier & 8-bit multiplier is

shown in figure 1 and 2.

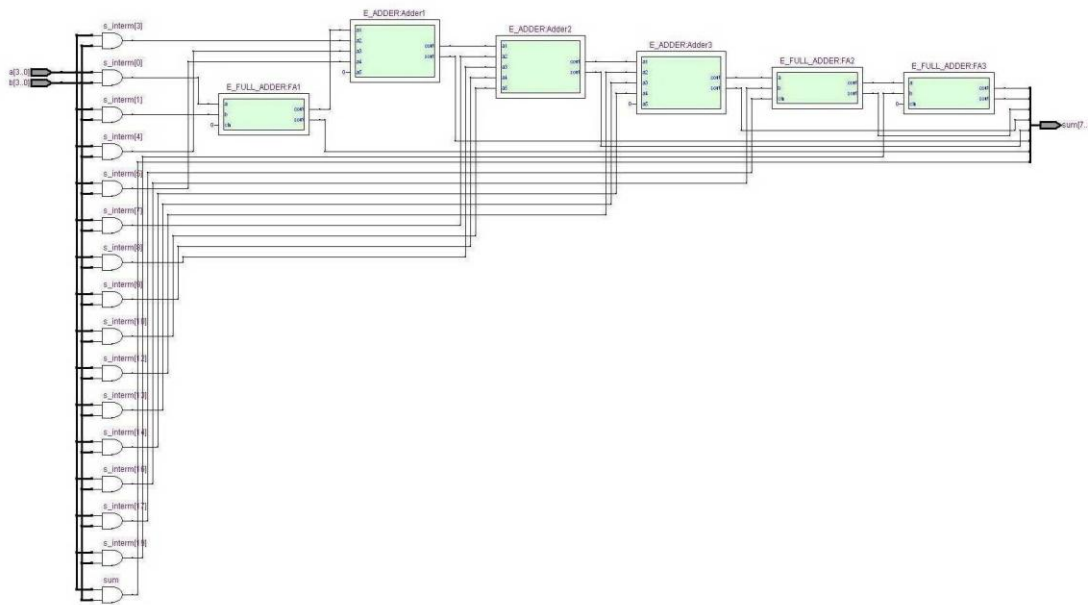


Fig. 1 RTL view of 4-bit multiplier block

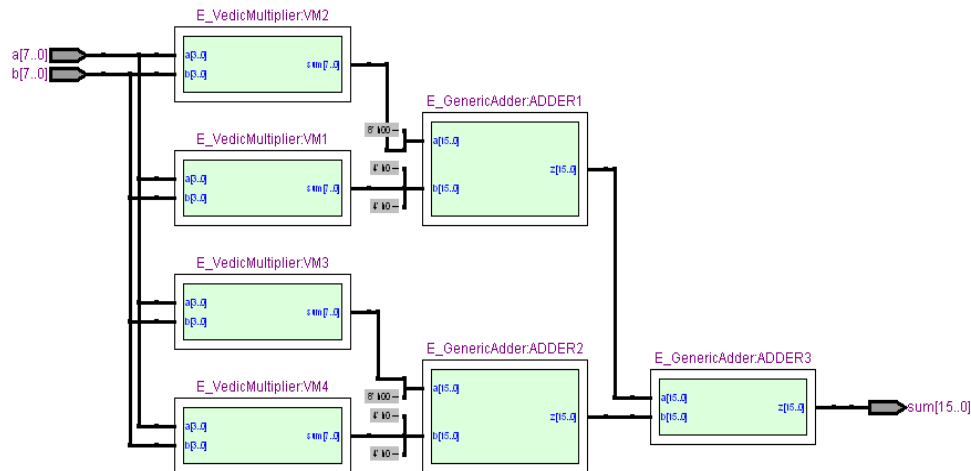


Fig. 2 RTL view of 8-bit multiplier block

V. Result and discussion:

- 1) For the implementation of 4 X 4 multiplier using Vedic mathematics input A is 2 (0010) and B is 7 (0111) then output of simulation is 14 (00001110).

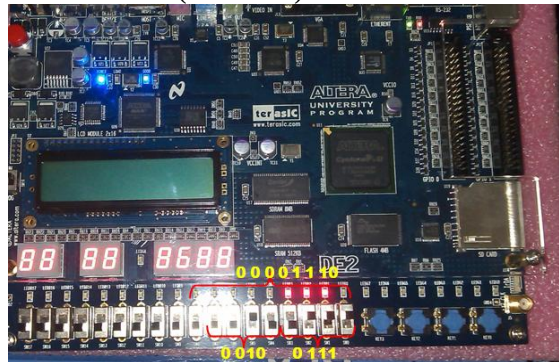


Fig. 3 LED output of 4 bit Multiplier on FPGA DE2 kit

- 2) For the implementation of 8 X 8 multiplier using vedic mathematics input A is 15 (00001111) and B is 10 (00001010) then output of simulation is 150 (10010110).

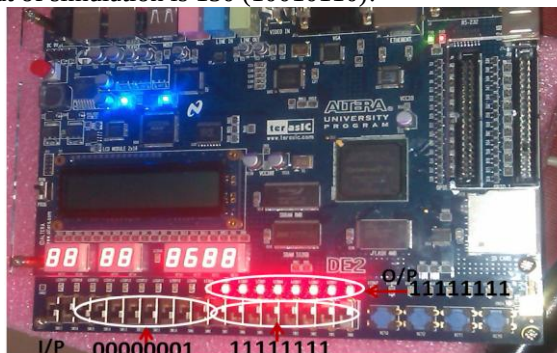


Fig 4. LED output of 8 bit Multiplier on FPGA DE2 kit

Type of Architecture	Method	Delay
4-Bit Multiplier	Conventional	12.75 ns
	Vedic	11.29 ns
8-Bit Multiplier	Conventional	27.312 ns
	Vedic	20.523 ns

Table 1 delay comparison

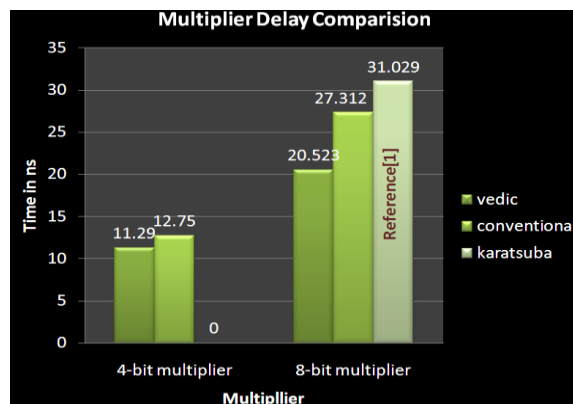


Fig. 5 Graph of delay comparisons

VI. Conclusion

- The design of 8 bit Vedic multiplier has been realized on Altera DE2 cyclone II FPGA kit. The computation delay for the 4 bit multiplier using vedic mathematics is 11.29 ns and it is 12.75 ns by the conventional method. 8 bit multiplier using vedic mathematics required computation delay 20.523 ns but multiplier using conventional method required computation delay 27.312ns which too much less.
- Finally, we can conclude that multiplier using Vedic mathematics is slightly positive in the areas of computation delay.
- Udrhva Tiryakbhayam Sutra is extremely efficient algorithm for multiplication as compare to conventional method for multiplier.

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