



DESIGN & IMPLEMENTATION OF DIGITAL DOWN CONVERTOR FOR WCDMA SYSTEMS

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Abstract: In this paper, we present Matlab implementation of a digital down convertor (DDC) for a single carrier WCDMA system. The implementation of DDC is simple and flexible due to use of FIR filters. In recent times, mobile communications need not only high data rate but also a relatively fast mobility. To implement a WCDMA system, one must address a number of key issues in signal processing related to implementation. Aiming at multi-channel IF signal processing requirements, DDC is designed and overall function diagram is given. The test on function and performance of multi-stage digital down converter system was conducted. Efficient design of DDC can contribute in the overall efficient system implementation. The DDC is designed for digital signal processing applications and wireless communication systems along with capability of flexible digital filtering.

Keywords—Digital up converter (DUC), Finite Impulse Response filter (FIR), Wide band Code Division Multiple Access (WCDMA), Cascaded Integrator and Comb filter (CIC), Intermediate Frequency (IF)

I. INTRODUCTION

DDC are extensively used in the radio systems. They are more popular than their analogue counterparts because of small size, low power consumption and accurate performance. The DDC converts the signal at the output of analog to digital convertor (ADC), centered at the intermediate frequency (IF), to complex baseband signal. In addition, DDC also decimates the baseband signal without affecting its spectral characteristics. The decimated signal, with a lower data rate, is easier to process on a low speed DSP processor. This paper discusses the DDC for the WCDMA system and implements them on the Matlab. WCDMA is a leading choice of data communication in the wireless industry nowadays and is selected as the air interface for the UMTS. WCDMA supports a higher data rate and is less susceptible to narrowband interferers and multipath fading. [1]. This paper discusses an efficient implementation of three stage DDC design for WCDMA to increase productivity and performance.

II. SYSTEM REQUIREMENTS

DDC must be designed to satisfy the 3rd generation partnership project (3GPP) specification which defines the transmission and reception required for base station radio of WCDMA.

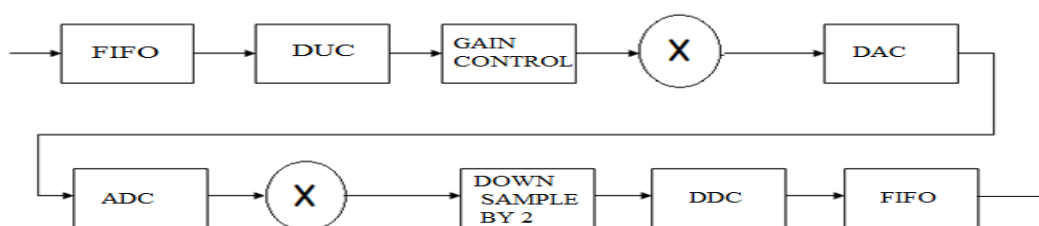


Fig 1 Front end block diagram for WCDMA[8]

DUC and DDC (Digital Down Converter) are integral part of a communication system, which are used to convert the sample rate of the signal. Digital up conversion is required when a signal is translated from baseband to intermediate frequency (IF) band. Digital down conversion is required when a signal is converted from IF band to baseband. In addition to sampling rate conversion, DUCs and DDCs typically include frequency shifting using mixers. The structure of a DUC or DDC depends mainly on the conversion ratio. For WCDMA systems, the conversion ratio is typically in the order of 8. DDC for WCDMA standard with decimation factor of 8 is designed. Fig 1 shows the top level front end lock diagram of WCDMA.[3] The WCDMA specification for uplink receiver path is given in Table 1.

Table 1. Specification for uplink receiver path[1]

Parameters	Values
Input signal quantization	14 bits

Output signal quantization	16 bits I & Q
Mixer properties	Tunability: Variable
IF sample rate	61.44 MCPS
No. of carriers	1
Carrier bandwidth	5 Mhz
DDC output rate	7.68 MSPS

III. DDC DESIGN

The DDC translates one or more intermediate IF channels from a set of specified center frequencies to 0 Hz. It also performs decimation and matched filtering to remove adjacent channels and maximize the received signal-to-noise ratio (SNR). The DDC input is assumed to be real, directly coming from the ADC. A simplified high-level block diagram of the WCDMA DDC is shown in Fig 2.

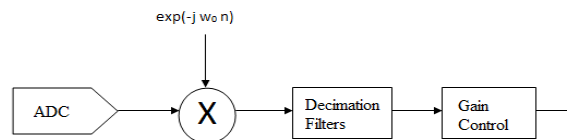


Fig 2 BASIC DDC[9]

DDC is an important component of a digital radio. It performs frequency translation to convert the high input sample rate down to a lower sample rate for efficient processing. The DDC accepts a bandpass signal with a sample rate around 70 (MSPS) and performs the following operations:

Digital mixing or down conversion of the input signal using a Numerically Controlled Oscillator (NCO) and a mixer. Narrowband low-pass filtering and decimation using a filter chain of Cascaded Integrator-Comb (CIC) and FIR filters. Gain is adjusted and final resampling of the data stream is done.

The DDC produces a baseband signal with a sample rate of 270 KSPS that is ready for demodulation.[2]

1. Frequency Translation

Frequency translation consists of mixer and DDS. The mixer translates the real input baseband signal from intermediate frequency to a complex baseband signal centered at 0 Hz.

2. CIC Decimation Filter

The CIC Decimation block performs a sample rate decrease (decimation) on an input signal by an integer factor. Cascaded Integrator-Comb (CIC) filters are a class of linear phase FIR filters comprised of a comb part and an integrator part.

3. Compensation Filter

The second filter of the conventional DDC compensates for the passband droop caused by the CIC. Since the CIC has a sinc-like response, it can be compensated for the droop with a lowpass filter that has an inverse-sinc response in the passband.

4. Lowpass Filter Design

Lowpass filter a discrete-time signal consisting of two sine waves. To obtain a complex bandpass filter, we translate lowpass decimator prototype to quarter sample rate by multiplying the filter coefficients with the heterodyne terms $\exp(-j\pi/2 \cdot n)$. Notice that while the coefficients of the lowpass filter are real, the coefficients of the translated filter are complex. The figure below depicts the magnitude responses of these filters.

Matlab model designed is shown in fig 3.

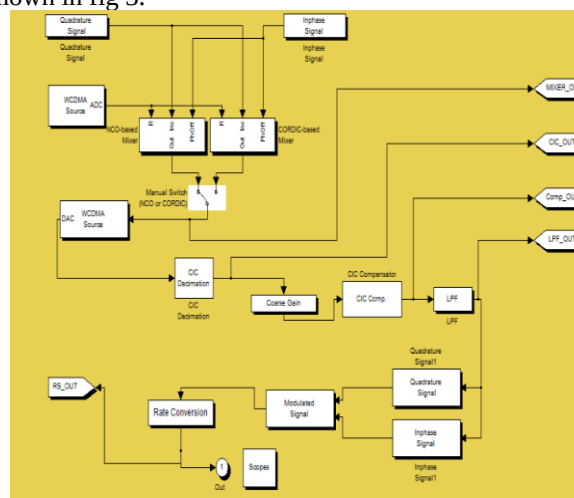


Fig 3 Matlab Model Design Of DDC

IV. RESULTS

The DDC is designed using Matlab. The following results are concluded.

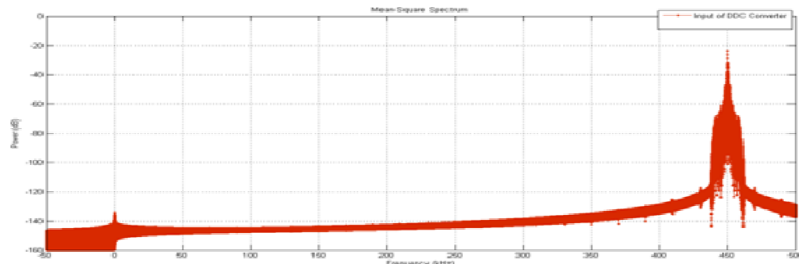


Fig 4 Input signal

The input DDC is shown in fig 4 .The input DDC is a 1 carrier WCDMA composite signal whose total power is set at the level of 30db below the desired signal.

The Periodogram block estimates the power spectral density or mean-square spectrum of the input. It does so by using the periodogram method and Welch's averaged, modified periodogram method. The block averages the squared magnitude of the FFT computed over windowed sections of the input. It then normalizes the spectral average by the square of the sum of the window samples. The block treats M -by- N frame-based matrix input and M -by- N sample-based matrix input as M sequential time samples from N independent channels. The block computes a separate estimate for each of the N independent channels and generates an N_{fft} -by- N matrix output.[10]

Each column of the output matrix contains the estimate of the power spectral density of the corresponding input column at N_{fft} equally spaced frequency points. The frequency points are in the range $(0, F_s)$, where F_s is the sampling frequency of the signal. The block always outputs sample-based data. Transmission of DDC is shown in fig 5 .

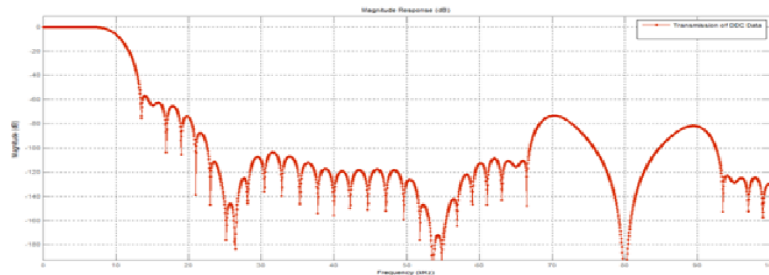


Fig 5 Transmission Of DDC

In statistical signal processing, the goal of spectral density estimation is to estimate the spectral density (also known as the power spectrum) of a random signal from a sequence of time samples of the signal. Intuitively speaking, the spectral density characterizes the frequency content of the signal. The purpose of estimating the spectral density is to detect any periodicities in the data, by observing peaks at the frequencies corresponding to these periodicities.

SDE should be distinguished from the field of frequency estimation, which assumes a limited (usually small) number of generating frequencies plus noise and seeks to find their frequencies. SDE makes no assumption on the number of components and seeks to estimate the whole generating spectrum. The output of DDC is shown in fig 6 .

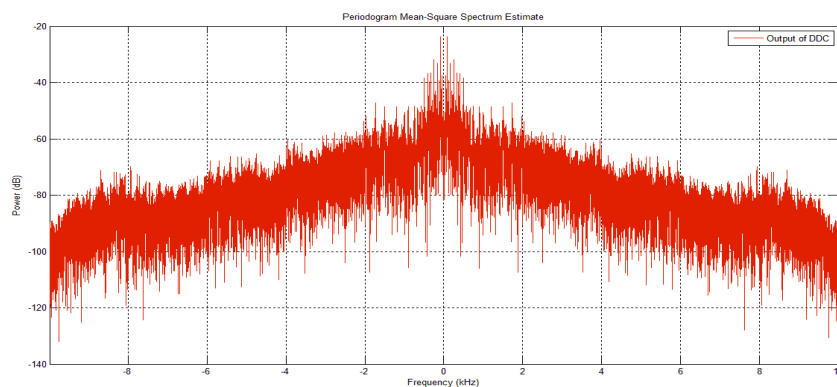


Fig 6 Output of DDC

This window estimates the power consumption with the frequency . The power consumption has been estimated in terms of db and the frequency has been estimated in terms of KHZ.The maximum power attained by this system is -20 db.

V. CONCLUSIONS

WCDMA is an emerging wireless communication system that can provide broadband access with large coverage area. In the present work an effort is made to reduce the cost of WCDMA system. From the study of literature related to WCDMA systems, it is concluded that DDC is the integral part of a WCDMA system and can provide further lead in improvement and up gradation. Study also shows that decimator filters required for DDC consumes significant hardware resources. So an efficient design in term of filter structure/configuration/architecture DDC can be implemented to an efficient and low cost WCDMA system for efficient and improved transmissions

As higher bandwidth can lead to more data rate and also design of digital systems at large bandwidth is of great challenge. So, in this thesis decimator stages of WCDMA DDC is designed for 5 MHz bandwidth. According to WCDMA standards, for 5 MHz channel bandwidth, DDC need to be designed for decimation factor of 8, and during their design, the spectral emission standards should be strictly followed..

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