



Enhancement of Tri-Model Switch for Low Power VLSI Application Using HDL

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Abstract: Power reduction is one of the biggest challenges in CMOS integrated circuit design. Optimization of power is inevitable in order to reduce package cost and extended battery life. As a switch tri-modal MTCMOS (Multi Threshold CMOS switch) can be considered as a low power solution for data retentive power gating applications. In MTCMOS, transistors with multiple threshold voltages are used in order to optimize power. The tri-modal switch provides three different power modes: active, drowsy and sleep. Drowsy mode has been introduced in this work which avoids the loss of data before the system going to sleep mode. The proposed system is useful for data-retention application which will replace the existing retention flip flops and thereby reduce the area.

Keywords: MT CMOS, active, drowsy, sleep mode, data retention

I. Introduction

Static power consumption and technology scaling plays an important role in CMOS integrated circuit design. While considering the static power consumption power density is a major factor. Power density increases due to the combination of higher clock speeds, smaller feature size and greater functional integration. Thus it becomes a greater challenge for the circuit designers. Even though the designers have a few methods for reducing this static power consumption, these methods have some drawbacks where one has to sacrifice design area and circuit performance. In this paper, we propose a new method to reduce static power in the CMOS VLSI circuit using a Tri-Modal Multi-Threshold CMOS Switch without being penalized in circuit performance.

Power optimization is very much important in reducing package cost and extending battery life. For power management, leakage power plays an important role in low power VLSI designs. Subthreshold leakage current is one of the major problem for battery-powered designs, and is becoming an increasingly fraction of overall power dissipation of ICs. Many low power designs require high performance while they are active and low leakage while idle. MTCMOS technology provides an excellent solution for this. The high performance requirement can be satisfied by low threshold transistors, which contributes excessive leakage current in the idle mode.

II. Related Works

In MTCMOS technology the selective application of multiple threshold voltages are employed which can maintain performance on critical paths with low threshold voltage (LVT) transistors while reducing leakage on other paths with high threshold voltage transistors (HVT). It is possible to turn off the power supply entirely for reducing idle leakage current in low-power designs. MTCMOS circuits use LVT transistors for computation and HVT transistors as a switch to disconnect the power supply during idle mode. There have been a number of studies on implementing on implementing low power modes. The work in [1] describes a power saving mode by placing HVT transistors between true V_{DD} and virtual V_{DDV} rails connected to the logic. A drawback of this arrangement is that the extra transistor increases the impedance between the true and virtual power supply which in turn cause greater power supply noise and gate delay.

The work in [4] proposes two intermediate power saving modes: drowsy and sleep mode. The idea is to add a clamping PMOS transistor in parallel with each NMOS sleep transistor. The circuit can be put into intermediate power saving mode by applying zero voltage to the gate of clamping PMOS and NMOS sleep transistors. Both leakage reduction and data retention can be achieved by this approach but we cannot ensure complete voltage swing. The voltage swing in [4] is from V_{DD} to $V_{DD} - V_{tp}$. The proposed method gives full voltage swing.

The work in [5] describes multiple power modes of low power circuit, but it requires additional supply voltages and therefore this method is costlier. Also this method is only suitable for applications with low standby period because sleep mode is lost in this configuration.

III. Proposed Work

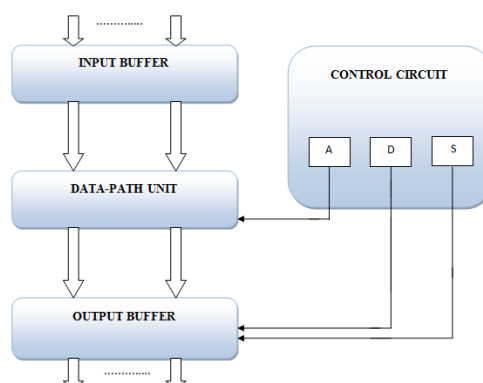


Fig. 1. Implementation of Tri-Modal system.

The circuit configuration shown in fig.1. consists of input buffer, data-path unit, control unit, and output buffer. The control circuit generates necessary control signals and depends on that, circuit may be either in active or drowsy or sleep mode. Drowsy mode is inserted for data retention capability, which is to avoid data loss before the system going to sleep mode. When the system is in active mode the data-path units processes the input data and generate corresponding output signals. In applications where the input data remains same, the system can be put into drowsy mode with data retention capability. Consider a cascaded network in which output of first stage drives the output of second stage and so on. At any particular time if the output does not depend on the output of preceding stage then that stage can be put into sleep mode. Thus power saving mode can be implemented.

A. Circuit Configuration and Technology

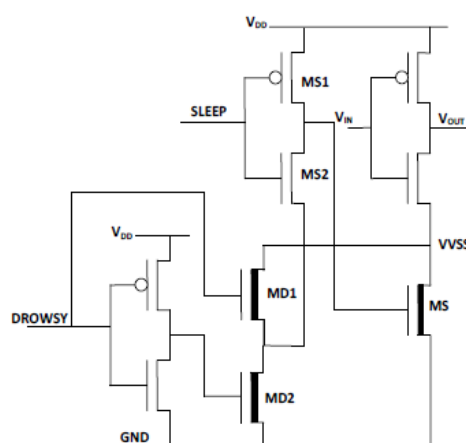


Fig.2. Tri-modal Footer cell Configuration

Data retentive tri-modal multi-threshold footer cell is shown in fig.2. The circuit block can be any circuit operating between V_{DD} and ground. The circuit can be switched between two power saving modes by using control inputs SLEEP and DROWSY. Transistors MD1, MD2 and MS are HVT (high threshold voltage devices) and the rest of the transistors are LVT (low threshold voltage devices). When SLEEP=1, the circuit will be in ACTIVE mode independent of the value of DROWSY control input. This is because when SLEEP=1, the PMOS device MS1 turns on and that leads to turn on the NMOS device MS. Therefore the VVSS node voltage is shorted to ground. Now the circuit block is operating in between actual V_{DD} and ground. Let us now discuss about the intermediate power saving DROWSY mode. When SLEEP=1 and DROWSY=1, both MS2 and MD1 turns on. Since the PMOS MS1 is off MS is also off. The transistors MS and MD2 are HVT devices and both are off and thereby cutting the ground supply rail. At the same time there exist a negative feedback path through the transistors MS2 and MD1, that causes small positive voltage at the node VVSS. This virtual ground supply rail voltage will be always greater than the actual ground potential when the circuit in DROWSY mode. In the normal operating condition (ACTIVE mode) the circuit is operating between V_{DD} and ground. In DROWSY mode the circuit is in between V_{DD} and VVSS. The voltage $V_{DD} - VSS$ is large enough to preserve the internal

data of the circuit; there is no need for data retention. The supply voltage has a quadratic relationship to the power dissipation. Therefore by reducing the supply voltage we can reduce the power dissipation.

$$P_{dynamic} = C_L V_{DD}^2 \propto f$$

When DROWSY=0 and SLEEP=1, the circuit will be in SLEEP mode. The HVT devices MS and MD1 are off and they limit the subthreshold leakage current of the circuit.

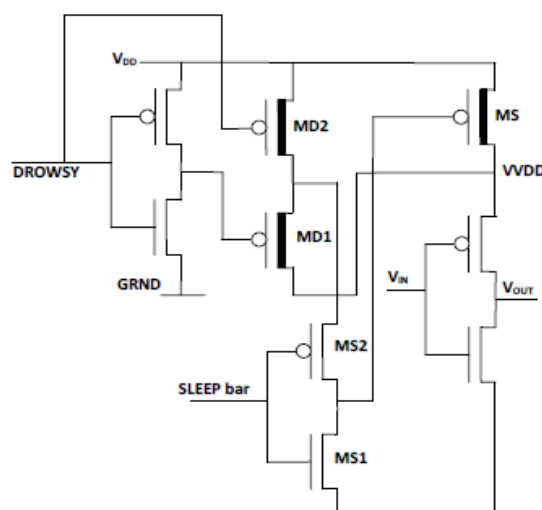


Fig.3. Tri-modal Header cell Configuration

Fig. 3 shows the header type tri-modal switch. The circuit configuration and functionality of tri-modal header is similar to the footer. The only difference is that the circuit block is operating between the virtual V_{DD} (VVDD) and actual ground, when the circuit is in DROWSY mode.

VVSS/VVDD is the virtual supply voltage that becomes important in the intermediate power saving DROWSY mode. From fig. 2 it is clear that the circuit is operating between V_{DD} and VVSS in DROWSY mode. The VVSS node voltage is the result of negative feedback through the transistors MS2 and MD1 in DROWSY mode. The voltage difference $V_{DD} - VVSS$ is large enough to preserve the internal data of the circuit without using data retention flip-flop. Both power and area can be optimized by this way. The value of the VVSS voltage depends on the channel width and threshold voltage of the NMOS transistor MS. Without VVSS voltage it is difficult to achieve drowsiness because we should suffer the area. An optional way is to use a data retention flip-flop at the output stage. But it consist of transmission gates and static inverters that are larger cells and introduces a significant amount of area overhead in designs that require data retention.

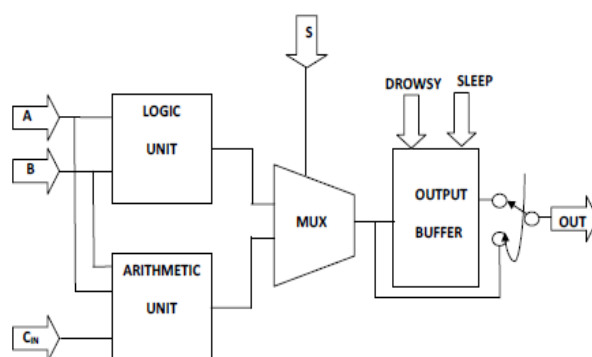


Fig.4. Tri-modal Data-retentive ALU

Data retentive tri-modal arithmetic and logic unit is shown in fig.4. ALU output can be selected by using a multiplexer. When the circuit is in active mode the inputs are processed inside the arithmetic or logic unit each time an event occurs. Then the multiplexer output can be directly passed as ALU output. In the drowsy mode output buffer is enabled with the help of DROWSY and SLEEP control signals and there is no need to process the input signals again. The previous output that was stored in the output buffer act as current ALU output. Thus

output data can be retained. When the SLEEP control is activated the ALU switches into power down sleep mode.

IV. Simulation Results

The functionality of tri-modal header and footer switches are verified by implementing an inverter in Mentor Graphics IC Station. Also we implemented a tri-modal ALU in Behavioral VHDL and synthesized the design using XST(VHDL\Verilog) compiler. We compared the power report of conventional ALU and the proposed tri-modal ALU and verified that the total estimated power consumption has been reduced from 9mW to 7 mW.

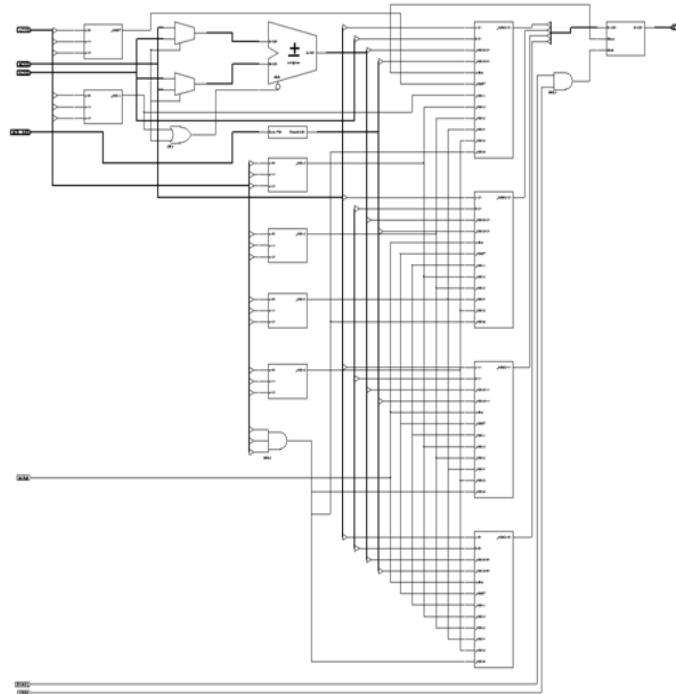


Fig.5. Top level schematic of Tri-modal data retentive ALU

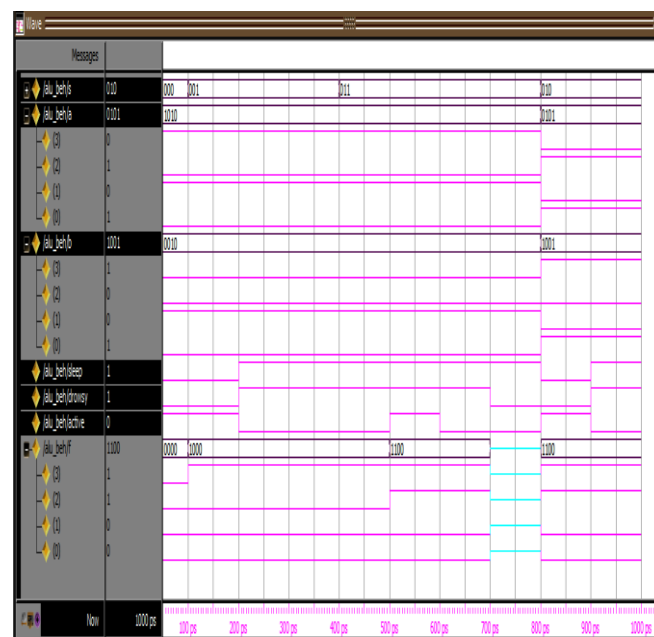


Fig.6. Output waveform of Tri-modal data retentive ALU

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		7
Vccint 2.50V:	0	0
Vcco33 3.30V:	2	7
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vcco33 3.30V:	2	7

Fig.7. Power summary of Tri-modal data retentive ALU

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		9
Vccint 2.50V:	1	3
Vcco33 3.30V:	2	7
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 2.50V:	1	3
Quiescent Vcco33 3.30V:	2	7

Fig.8. Power summary of Conventional ALU

V. Conclusion

We presented a data retentive low power solution for VLSI applications by using a Tri-modal switch. We implemented three power saving modes: active, drowsy and sleep in inverter circuit and verified the switch functionality. A data retentive tri-modal ALU is designed in behavioral VHDL and synthesized the design using XST compiler and showed that the total estimated power consumption has been significantly reduced. The proposed Tri-modal switch can be used for a wide range of data retentive applications.

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