



VLSI ARCHITECTURE FOR DISCRETE WAVELET PACKET TRANSFORM USING CSD TECHNIQUE

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Abstract: The proposed paper presents multiplier-less architecture for the discrete wavelet transform using canonic signed digit (CSD). In the proposed architecture, the canonic sign digit (CSD) algorithm has been applied to reduce the number of full adders required by 2's complement based designs. The proposed design has been coded in VHDL and functionality is verified by RTL and gate level simulation targeting Xilinx vertex-IV, SF Packet 363. The proposed architecture is based on arithmetic for low complexity and efficient implementation of 2-D discrete wavelet transform. DWPT provides good temporal and spectral resolutions in arbitrary regions of the time and frequency plane. With this proposed architecture the speed of the 2-D DWPT operation will increase. This architecture is suitable for high speed on-line applications.

Keywords: Discrete wavelet packet transform (DWPT), One, Two, Three Level, Canonic signed digit (CSD) scheme

I. Introduction

Among many discrete cosine transform (DCT) and discrete sine transform (DST), discrete wavelet transform (DWT) have numerous applications such as speech analysis, image coding, computer vision and so on. The DWT can decompose a signal into a number of frequency bands [1]. Wavelet provides an alternative to the time-frequency representation in signal processing domain. The shifting (or translation) and the scaling (or dilation) are unique to wavelets. The wavelet is a kind of bases which are generated by dilation and translation of a function [1], [2]. The wavelet analysis method has a good ability to localize signal in both time and frequency plane [4]. DWPT has also been widely used in many applications, especially in image and video coding, speech and audio coding, speech enhancement, speech recognition, hearing aid, digital computation, medical and fingerprints [2], [3], [4].

In this paper, the bit-level multiplication of two number can be performed by shift and add operation in the simplest form. It has been observed that the complexity of a shift-add type signed multiplier is depends on the number of one's of the 2's complement representation of the multiplicand number with the shifted partial sum whereas the zeros will only shift the partial sum. It is assumed that the shifting does not required any hardware as it can be done by hardwiring. The number of one's of the 2's complement number, therefore, will determine the numbers of full adder (FA) required in implementation of the multiplier. Canonic signed digit (CSD) are popular for representing a number with fewest number of non-zero digit.

No 2 consecutive bits in a CSD number are non-zero.

The CSD representation of a number contains the minimum possible number of nonzero bits, thus the name canonic.

The CSD representation of a number is unique.

CSD numbers cover the range $(-4/3, 4/3)$, out of which the value in the range $\{-1, 1\}$ are of greatest interest.

The CSD number has 33% fewer average non-zero bits than 2's complement number.

In the DWT, each level is calculated by passing the previous approximation coefficients through a high and low pass filters. However, in DWPT, both detail and approximation coefficients are decomposed [5]. Comparing the 2-D DWT with the 1-D DWT, we find that in the 1-D DWT the range of operation is halved with a change in decomposition level j , while in the 2-D DWT the range of operation is always the whole frame. So as the operation range halved with the increase in decomposition level, the above structure can perform the 1-D DWT easily.

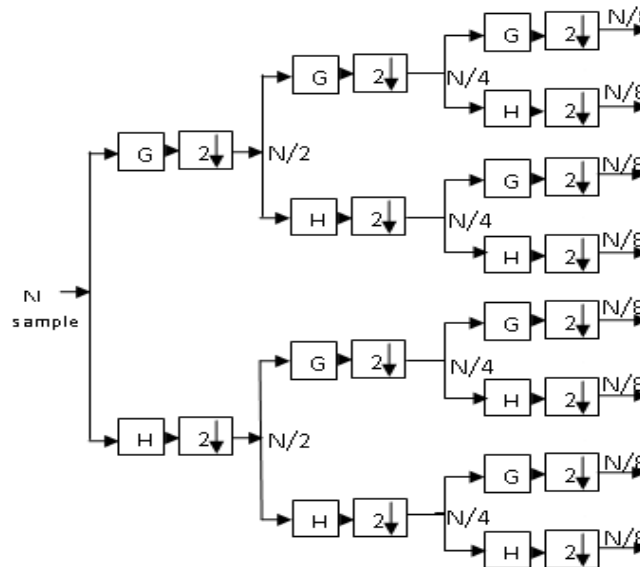
This paper proposes, a new CSD based architecture for the 2-D Discrete wavelet packet transform. The rest of the paper is structured as follows: Section II describes the algorithm for the tree structure of wavelet packet transform. Section III describes the low complexity design for DWPT. Section IV describes CSD based design for DWPT. Section V describes the proposed architecture for CSD based design for DWPT. In Section VI and VII, conclusion and simulation result is given.

II. Direct Wavelet Packet Transform

The tree structure of 2-D Discrete Wavelet Packet Transform (DWPT) is based on the filtering process [6]. Computation period is the number of the input cycles for one time produces output samples. In general, the computation period is $M=$ for a j -level DWPT. The period of the 3-level computation is 8. Figure 1 describes the complete 3-level decomposition for DWPT, for example, suppose that the original signal $X[n]$ has N - sample points, spanning a frequency band of zero to π rad/s. At the first decomposition level, the signal passed through the high pass and low pass filters, followed by sub- sampling by 2. The output of the high pass filter has $N/2$ -sample points (hence half the time resolution) but it only spans the frequencies $\pi/2$ to π rad/s (hence, double the frequency resolution).

The output of the low-pass filter has also $N/2$ - sample points, but it spans the other half of the frequency band, frequencies from 0 to $\pi/2$ rad/s. Again low and high-pass filter output passed through the same low pass and high pass filters for further decomposition. The output of the second low pass filter followed by sub sampling has $N/4$ samples spanning a frequency band of 0 to $\pi/4$ rad/s, and the output of the second high pass filter followed by sub sampling has $N/4$ samples spanning a frequency band of $\pi/4$ to $\pi/2$ rad/s. The second high pass filtered signal constitutes the second level of DWPT coefficients. This signal has half the time resolution, but twice the frequency resolution of the first level signal. This process continues until two samples are left. For this specific example there would be 3 levels of decomposition, each having half the number of samples of the previous level. The DWPT of the original signal is then obtained by concatenating all coefficients starting from the last level of decomposition.

Figure1: Complete 3-level decomposition for DWPT



In this figure, G is high pass filter and H is low pass filter.

III. Low Complexity Design for DWPT

In DWT, only the outputs of the low-pass filters are further processed at the next level, while the outputs of the high- pass filters remain as final results. While in 2-D DWPT allows further processing of both the outputs of low and high-pass filters at the next level that gives flexibility to arbitrary decomposition on time and frequency plane. DWPT computation is nothing but two-channel FIR filter computation. Low-pass and high-pass down sampled filter computations are performed on the input to calculate the DWPT coefficients. Low-pass down sampled filter is the average between two samples and high-pass filter is the difference between two samples. The DWPT algorithms for 1-level decomposition are given as;

$$Y_{high}[k] = \sum_n h[n] * x[2k - n] \quad (1)$$

$$Y_{low}[k] = \sum_n g[n] * x[2k - n] \quad (2)$$

Where, $x(n)$ is the input and $Y_{high}[k]$ & $Y_{low}[k]$ are low-pass and high-pass DWPT coefficients respectively, $h[n]$ and $g[n]$ are low-pass and high-pass filter coefficients respectively. Daubechies four tap (Daub-4) filter coefficients are assumed for the low-pass filter proposed design. However, similar type of design can be derived for other type of wavelet filters as well. The Daub-4 low-pass filter coefficients are taken [8]. The corresponding high-pass filter coefficients are calculated using the following relation:

$$g(n) = (-1)^k h(N - n) \quad (3)$$

Where, $h(n)$ and $g(n)$ are low and high-pass filter coefficients respectively. N is the filter order.

Table1: Low and high-pass Daub-4 filter coefficients. The binary digit 1 shown in bold face represents - 1 of the CSD digit

Filter Coefficient	Decimal representation	2's Complement representation	CSD representation
h(0)	0.4829629131	0.01111011	0.10000 1 00
h(1)	0.8365163037	0.11010110	1.00 1 01010
h(2)	0.2241438680	0.00111001	0.0100 1 010
h(3)	-0.129409522	1.11011110	0.00 1 0000 1
g(0)	-0.129409522	1.11011110	0.00 1 0000 1
g(1)	-0.224143868	1.11000110	0.0 1 001010
g(2)	0.836516303	0.11010110	1.00 1 01010
g(3)	-0.482962913	1.10000100	0. 1 0000100

The 8 bit 2's complement and CSD representation of the low and high-pass filter coefficient are given in above table1. Equation can be rewritten four-tap FIR filter as:

$$Y_h[k] = [h(0) + h(1)Z^{-1} + h(2)Z^{-2} + h(3)Z^{-3}] X(n) \quad (4)$$

$$Y_l[k] = [g(0) + g(1)Z^{-1} + g(2)Z^{-2} + g(3)Z^{-3}] X(n) \quad (5)$$

Where, Z^{-1} operator represents one sample delay in Z-domain.

IV. CSD Based Design for DWPT

Canonical Signed Digit (CSD) is multiplier-less architecture. Each of the multiplier unit is replaced with shifters and adders/subtraction for CSD implementation of DWPT. The constant multiplication factors of (4) and (5) are replaced with shift and adder/subtraction operation and rewritten as below:

For low pass filter:-

$$Y_h[K] = [x(n) \gg 1 - x(n) \gg 6 - x(n) \gg 9] + [-x(n-1) \gg 3 - x(n-1) \gg 5 - x(n-1) \gg 7] + [x(n-2) \gg 2 - x(n-2) \gg 5 + x(n-2) \gg 7] + [-x(n-3) \gg 3 - x(n-3) \gg 8] \quad (6)$$

For high pass filter:-

$$Y_g[K] = [-x(n) \gg 3 - x(n) \gg 8] + [-x(n-1) \gg 2 + x(n-1) \gg 5 - x(n-1) \gg 7] + [-x(n-2) \gg 3 - x(n-2) \gg 5 - x(n-2) \gg 7] + [-x(n-3) \gg 1 + x(n-3) \gg 6] \quad (7)$$

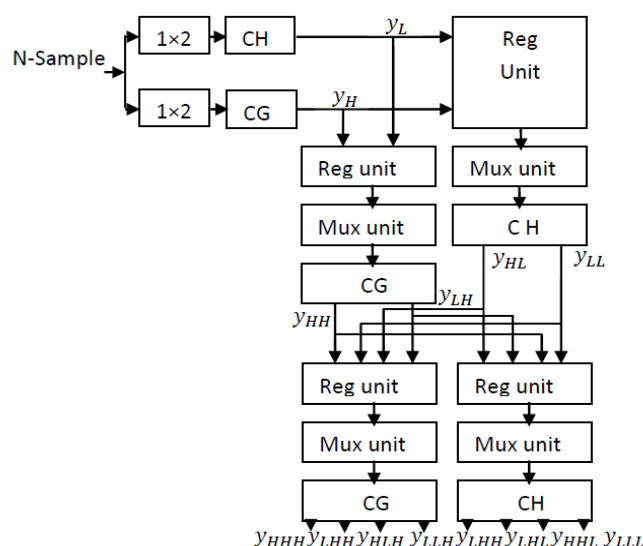
V. Proposed Architecture

For the real-time VLSI implementation of DWPT, this paper presents a CSD (canonic signed digit) based architecture. The CSD architecture has the number of add operations required in a constant coefficient multiplication equals one less than the number of nonzero bits in the constant coefficient. In order to further reduce the area and power consumption, the constant coefficient can be encoded such that it contains the fewest number of nonzero bits, which can be accomplished by using CSD representation.

The operation of the architecture is describes as follows: The original signal $X[n]$ has N - sample points, is passed through 1×2 demultiplier. When selection line is 0, even samples are formed and when selection line is 1, odd samples are formed. After that passed these samples through CSD based low-pass filter, same process with high-pass filter. At the first decomposition level, the output of CSD based high-pass (Y_H) and low-pass filter (Y_L), $N/2$ samples are obtained. At the second decomposition level, the output of CSD based low-pass and high-pass filter are passed. Now, the output passed through mux. When the selection line is 0, output of CSD based low-pass filter is obtained and when the selection line is 1, output of CSD based high-pass filter is obtained and after that mux output passed through CSD based low-pass filter which gives Y_{LL} & Y_{LH} output. Same process is applied with the CSD based high-pass filter which gives Y_{HL} & Y_{HH} output. At the third decomposition level, the time period is doubled and frequency will be halved, and the output of CSD based low and high pass filter is passed through a register unit and then passed through mux. When selection line is 00, CSD based low-pass filter output Y_{LL} is obtained and when selection line is 01, Y_{LH} is obtained. When select line is 10, Y_{HL} is obtained and when selection line is 11, Y_{HH} is obtained. And finally, mux output passed through CSD based low-pass filter, $Y_{LLL}, Y_{LHL}, Y_{HLL}, Y_{HHL}$ are obtained and when passed through high-pass filter, $Y_{LLH}, Y_{LHH}, Y_{HLH}, Y_{HHH}$ are obtained.

Figure 2: Complete 3-levels for DWPT

Where, CG and CH are the CSD based high-pass and low-pass filters respectively



VI. Performance Evaluation

The proposed architecture of canonic signed digit based (CSDB) for DWPT is obtained by different approaches, in which Xilinx9.2i is used for simulation. These simulation results are then used in the VHDL simulation to evaluate the performance of the DWPT.

Table2: Multiplier based technique

Decomposition Level	Multiplier	Adder	No. of slices	No. of 4 LUTs	Required time (nsec)
First	8	6	136	247	11.129
second	16	12	355	654	18.345
Third	24	18	613	1114	25.568

Table3: Proposed architecture (CSD based technique)

Decomposition Level	Multiplier	Adder	No. of slices	No. of 4 LUTs	Required time (nsec)
First	-	30	49	89	8.920
second	-	60	67	121	10.565
Third	-	90	141	252	8.018

The result is shown in Table 2 and Table 3. In CSD based technique, requirement of multiplier is zero and no. of slices, no. of 4LUTs, time requirement is also reduced as compared to multiplier based technique. And if no. of slices is less then area will be reduced and hence, automatically time will also be reduced in CSD based technique. This is the main advantage of proposed architecture.

VII. Conclusion

This paper presents multiplier-less (CSD) based design. In the proposed architecture, canonic signed digit (CSD) number system is used to represent the filter coefficients of the wavelet filter with minimum no. of ones. In this architecture, use of low-pass filter is the average between two samples and high-pass filter is the difference between two samples. With this architecture, the speed of wavelet packet transform is increased, occupied area of circuit is reduced about 50% and power requirement is reduced about 15-25% of previous convolution based architecture. It has 100% hardware utilization efficiency.

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