

Low Power Operational Amplifier

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Abstract— For low power circuit. Circuit work at the low voltage supply, but at low voltage supply Integrated circuit designers start to face a power wall as the most difficult constraints. In new technology and large demand in market of portable electronic equipment are increasing the interest in very low power integrated circuits. Designing very low power integrated circuits requires the reduction of the internal power supply voltages and interconnection parasitic element should be minimum, as these are the most important parameters associated to power dissipation. For maintain the circuit performance at low voltage supply reduced the threshold voltage of the transistor which impose a large number of serious problem both in circuit design and technology. After decrease the threshold voltage the margin for error decrease and circuit parameter dramatically degrade the performance of original circuit. In this paper we used current compensation technique to minimize the power consumption.

Key word: AC analysis, DC analysis Transient analysis gain, power dissipation, 180nm technology, cadence.

I. Introduction

Here we use current compensation technique to minimize the power consumption here we design the operational amplifier using cadence 180nm technology and 65 nm technology and calculate the gain and power consumption.

A basic operational amplifier consists of 4 main blocks [14]

- Dual input Differential output
- Differential input single ended output
- Level shifter
- Output buffer

figure 1 The general structure of operational amplifier



II. Implementation and Result

Here we implemented the operational amplifier using current compensation technique in cadence at 65nm and 180nm technology. Figure shows below the schematic diagram of operational amplifier.

Figure 2 schematic diagram of operational amplifier

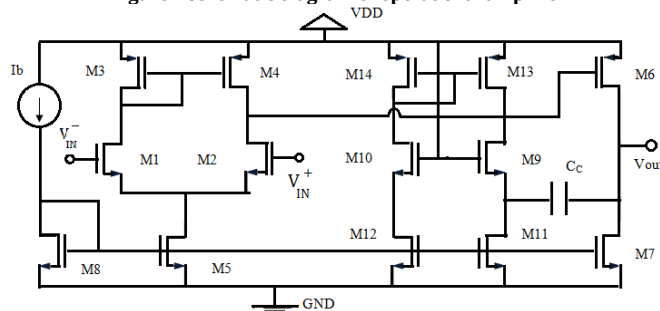


Figure 3 schematic diagram of op-amp using 180 nm technology

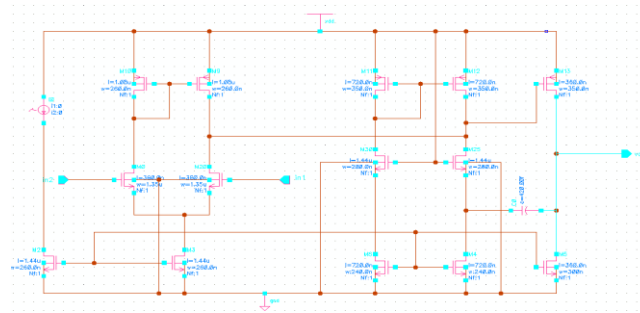
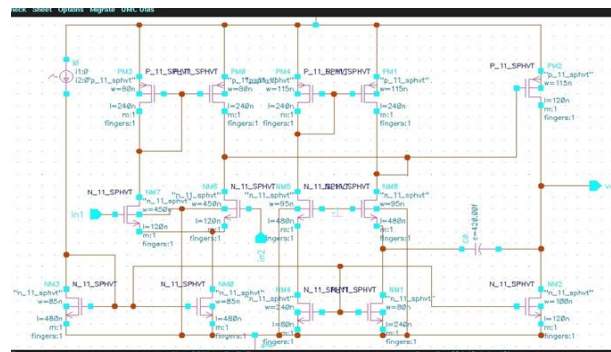


Figure 4 schematic diagram of op-amp using 65nm technology



Transient analysis of op-amp

Figure 5 input and output of op amp at 180nm technology

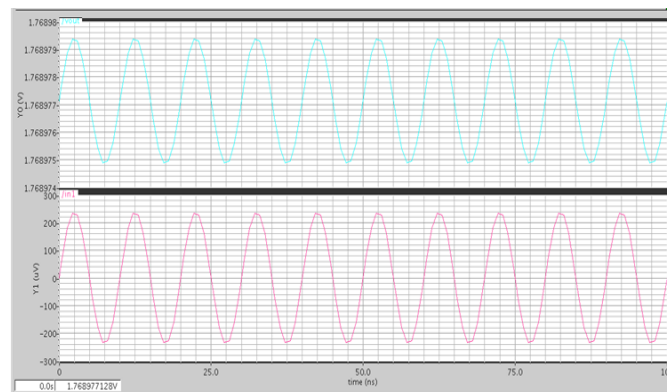


Figure 6 input and output of op-amp at 65 nm technology

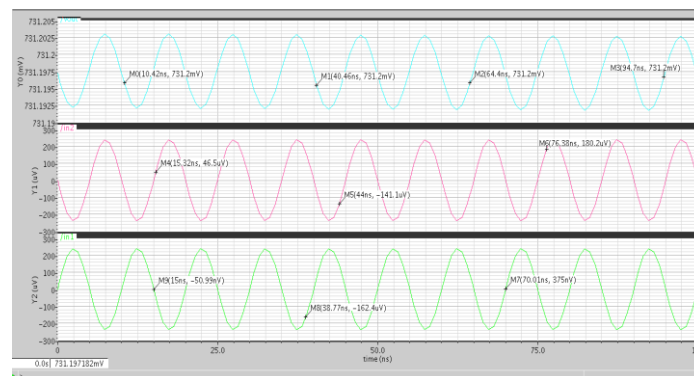


Figure 7 Slew rate of op-amp at 180nm technology

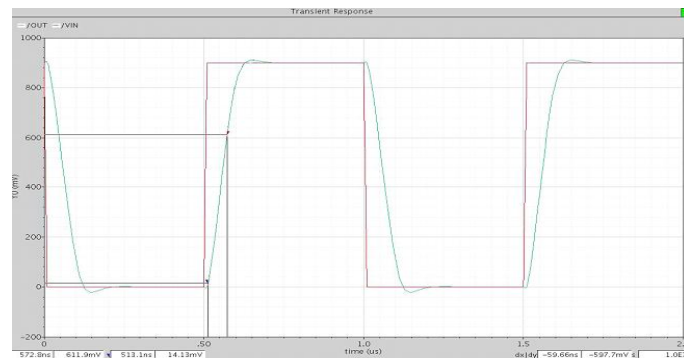
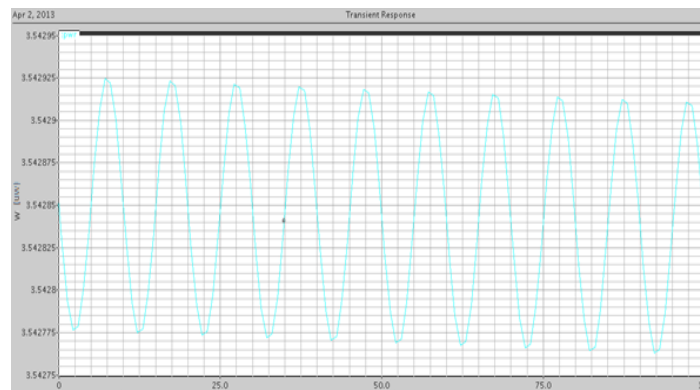
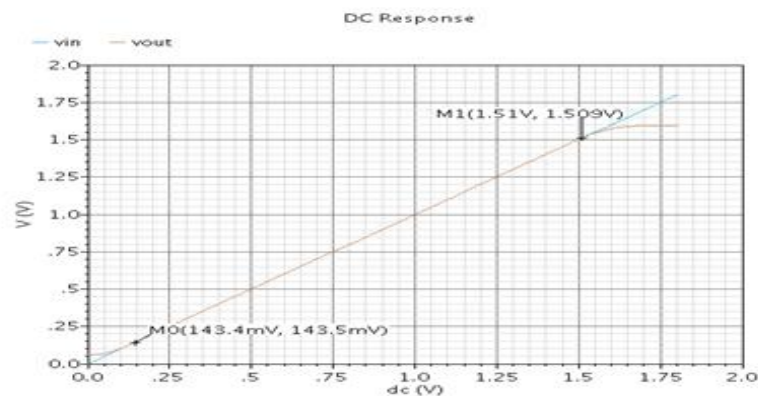


Figure 8 Power dissipation graph at 180nm technology



DC analysis

Figure 9 ICMR of op-amp at 180nm technology



AC analysis

Figure 10 gain and phase diagram 180nm technology

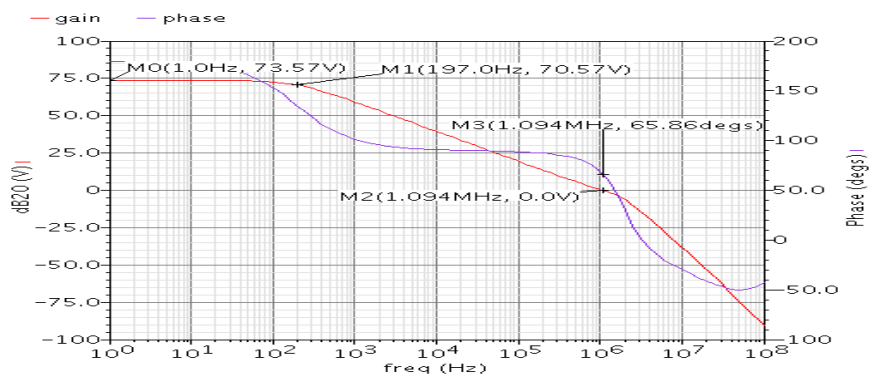
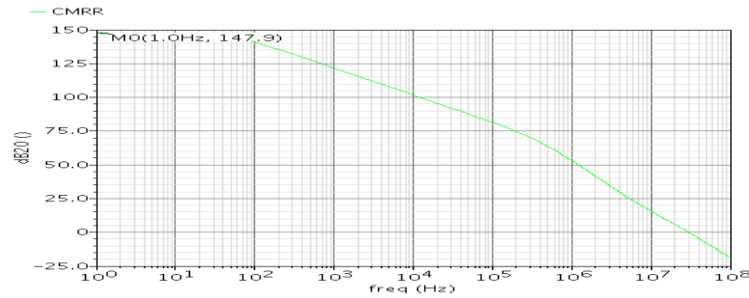


Figure 11 graph of CMRR at 180nm technology



III. SIZE OF TRANSISTOR

Table 1 size of transistor of 65 nm and 180 nm technology

TRANSISTOR	SIZE(W/L) .18 μ m(μ m/ μ m)	SIZE(W/L) 65nm(nm/nm)	TYPE
M1,2	1.35/.36	450/120	NMOS
M3,4	.26/1.05	80/240	PMOS
M5,8	.26/1.44	85/480	NMOS
M6	.35/.36	115/120	PMOS
M7	.30/.36	100/120	NMOS
M9,10	.28/1.44	80/480	NMOS
M11,12	.24/.72	80/240	NMOS
M13,14	.35/.72	115/240	PMOS
C _c	.420pf	.420pf	

Table 2 Comparison between Simulated Result and Previous Paper Result

Characteristics	[2]	[3]	[4]	[5]	[7]	[8]	This Work
Supply Voltage (V)	3	1.5	1.5	2	1.5	0.8	1.5
DC Gain (dB)	20.88	80	82	102	48	51	73.57
UGB (MHz)	15.4	167	1.15	0.48	NA	0.057	1.084
PM (Degree)	-19.6	73.5	86	60.35	NA	60	65.89
Slew Rate + (V/ μ S)	NA	464	0.73	0.20	NA	0.14	10.1
Slew Rate - (V/ μ S)	NA	NA	0.73	0.21	NA	NA	-9.5
ICMR (V)	NA	1.13	NA	-0.35 to 1.13	NA	NA	0.143 to 1.51
Offset Voltage (μ V)	50	NA	NA	0.25	NA	NA	NA
PSRR	NA	NA	NA	59.7	NA	NA	92.95
CMRR (dB)	-53	NA	NA	102.004	NA	NA	147.9
Power Dissipation	570(μ w)	8.9(mw)	NA	25.745(mw)	6.5(mw)	1.2(uw)	3.54(uw)

IV. Conclusion

This paper present a new low power operational amplifier circuit operating with the supply voltage 1.5v and power dissipation is 3.54(uw). proposed circuit can be used for wide verities of low voltage and low power application. The simulation result having presented to demonstrate the feasibility of the proposed low power operational amplifier circuit.

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