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DESIGN of a TIQ COMPARATOR for HIGH SPEED and LOW POWER 4 BIT FLASH ADC

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Abstract: The area of low power and high speed designing of analog-to-digital converters (ADCs) has been a challenging issue over the last decade. The speed enhancement of serial links and the emerging communication technologies has inclined many researchers towards improvement of power and speed specifications. The major building block governing these specifications is the comparator. This paper deals with a new design for comparator with threshold inverter quantization (TIQ) technique. The TIQ technique uses two cascaded CMOS inverters as a voltage comparator. In this design the threshold voltage is used as a reference for comparing the input voltage. The proposed paper introduces TIQ comparator for a flash A/D converter. The TIQ based flash ADC requires $2^n - 1$ comparators. The proposed comparator design provides high speed, low power consumption and smaller area. The simulation is performed on Tanner tool with $0.25\mu\text{m}$ technology.

Keywords: TIQ; flash ADC; low power; inverter; pass transistor

I. INTRODUCTION

The processors and ADC designs these days demand high speed operation and less power consumed architecture. Various architectures of ADC have been proposed by researchers during the last decade with different resolutions, sampling rates, power consumptions and temperature ranges. These ADCs are used in different applications from mobile communication devices to measure equipment [1]. Since the performance parameters like sampling rate, resolution, and power consumption of an ADC is basically determined by its architecture, one single ADC type cannot cover all applications [3]. Therefore, it is important to properly choose an ADC for each particular application. One of the commonly used ADC is flash type ADC because of the better tradeoff between its performance metrics.

For instance, a flash (parallel) type ADC architecture is mainly used for high speed and low resolution applications. A flash ADC comprises of two basic building blocks: comparators and encoder. Comparator block is used for comparing the input signal with the reference signal and generated thermocode value and encoder is used for converting thermocode values in to digital output.

Flash ADC is not efficient for the resolution of more than 8-bit. As long as resolution level is kept large, the comparator count will be reasonable. Therefore the comparator is more critical part of flash ADC. In this paper author proposes small size and low power consumed TIQ comparator. TIQ comparator uses two cascading CMOS inverter for comparing input analog signal with internal reference voltage and generate corresponding digital output. In this comparator threshold voltage is used as an internal reference voltage which consequently eliminates the need of resistor ladder circuit from flash ADC.

Flash ADC requires $2^n - 1$ different size comparators for the generation of thermocode. Here TIQ comparators are designed which uses two cascading inverters as a voltage comparator. The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters [4]. Hence, we do not need the resistor ladder circuit used in a conventional flash ADC. The second stage inverter is the gain booster, which makes a sharper threshold for comparator outputs and provides full digital output voltage swing. In a conventional flash ADC, reference voltage is generated using a resistor ladder circuit [5]. Due to resistor ladder circuit the size of comparator is large and also consumes more power. Some of the main problems of the conventional comparator structure are [2].

1. Large area for high accuracy
2. DC biasing requirement
3. Charge injection errors
4. Metastability error
5. High power consumption
6. Resistor array required.

These problems can be overcome by using TIQ technique.

II. TIQ COMPARATOR

The comparator is the most important part in the ADC architecture whose role is to convert input voltage V_{in} to logic 1 or 0. The voltage comparators compare the input voltage with internal reference voltages, which are

determined by the transistor sizes of the inverters. TIQ comparator is basic CMOS inverter which comprises of one PMOS and one NMOS transistor with the switching threshold voltage [5]. The TIQ comparator consists of the two cascaded CMOS inverter where the first inverter is used for setting the reference voltage of comparator by varying the width and length of the PMOS and NMOS transistors, whereas the second inverter is used for increasing the voltage gain of the comparator and manages the propagation delay in balance [2]. As the threshold voltage is a direct function of size i.e. length and width of the transistor, one has to vary either the length or the width to get a better performance. But on the other hand the change in the length of the transistor is having a sensitive and significant effect on the threshold voltage which can severely affect the performance and even lead to unstable response. So the width is varied to change the threshold voltage to get a suitable range of variation. Two cascaded inverters and their switching voltages are shown in figures 1 and 2 respectively.

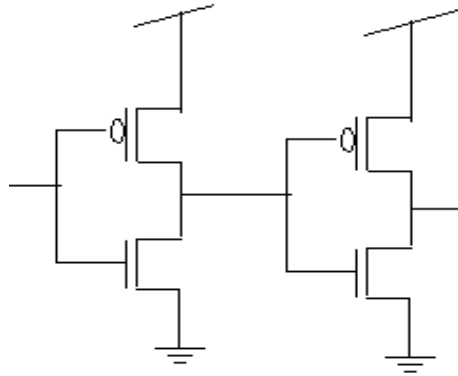


Figure 1. TIQ schematic diagram

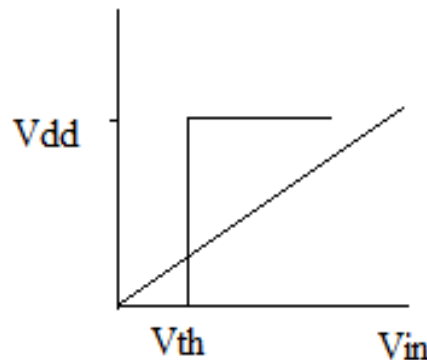


Figure 2. TIQ characteristic

The second stage is exactly same as first stage to maintain the same DC threshold level and to keep the linearity in balance for voltage variations of high frequency inputs [3]. The threshold voltage (V_{th}) governing the switching characteristics of a CMOS inverter can be approximately given by the following equations [7].

$$V_{th} = \frac{|V_{tp}| + V_{tn} \sqrt{\frac{K_n}{K_p}}}{1 + \sqrt{K_n + K_p}} \quad (1)$$

$$K_n = \frac{W}{L}_n \mu_n c_{ox} \quad (2)$$

$$K_p = \frac{W}{L}_p \mu_p c_{ox}$$

Where V_{tp} and V_{tn} are the threshold voltages of PMOS and NMOS transistors respectively and μ_p and μ_n are the mobilities of PMOS and NMOS transistors respectively.

The TIQ comparator generates a sharper threshold for comparator output and provides a digital output voltage. The propagation delay is almost exponentially proportional to the transistor length but voltage gain followed logarithmic function, therefore propagation delay and voltage gain both are considered in the transistor sizing of the TIQ comparator [1].

The TIQ techniques have many advantages like [4]:

1. Simple voltage comparator circuit
2. Faster voltage comparison speed
3. Elimination of resistor ladder circuit
4. Does not required clock signals or coupling capacitor for the voltage comparison

III. CALCULATION AND CONSIDERATION OF TIQ COMPARATOR

It has been stated earlier that a TIQ comparator generates reference voltage internally; the length and width of PMOS and NMOS are varied in order to obtain desired switching voltage [2]. Here the comparator switching voltage is depending on the threshold voltage of PMOS and NMOS. To reduce power consumption of the design, the threshold voltage should not be deviated too much. In contrast, even if the transistor length is kept very small to attain a high speed, it will affect the output because of the channel noise and results in a nonlinear switching pattern. Therefore the length of the transistor is kept fixed at a nominal value and width of transistor is used for generating different switching voltages. In this design low leakage current MOS devices are used in order to keep the power consumption as small as possible, keep $W_p / W_n < 1$ to reduced power consumption and also to reduced parasitic capacitance.

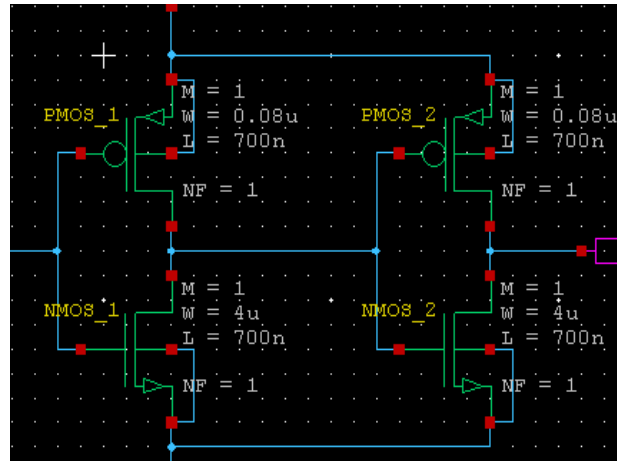


Figure 3. Schematic of TIQ comparator

In the proposed design the size of the NMOS and PMOS with their minimum and maximum switching voltages are shown in table 1. Different switching voltages are obtained by varies W_p and W_n as given in figure 4. The table shows the variation of W_p and W_n on the switching voltage. W_p is first decreased for a constant W_n to get its effect on switching voltage and then W_n is decreased for a constant W_p . The variation of switching voltage in the table 1 given below clearly shows that it is minimum for $W_p=0.23\mu\text{m}$ and $W_n=4\mu\text{m}$.

Table no. 1

Comparator no.	W_p (μm)	W_n (μm)	Switching voltage (V)
1	0.23	4	0.43
2	0.03	4	0.49
3	0.045	4	0.52
4	0.08	4	0.57
5	0.18	4	0.6
6	0.4	4	0.62
7	1.6	4	0.68
8	4	4	0.71
9	4	1.6	0.76
10	4	0.8	0.80
11	4	0.4	0.83
12	4	0.2	0.88
13	4	0.1	0.91
14	4	0.075	0.97
15	4	0.06	0.99

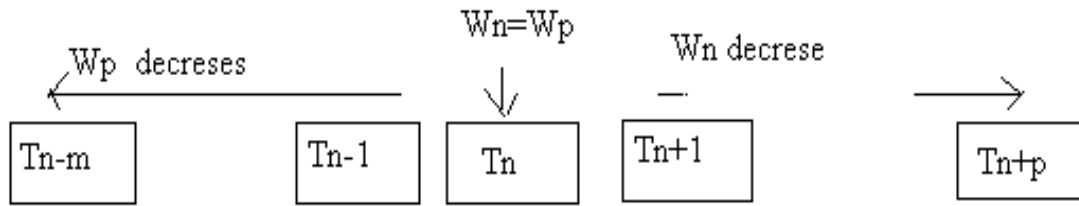


Figure 4. Transistor width variations

IV. SIMULATION RESULTS

Simulation of the design is performed using 0.25 μ m CMOS technology in Tanner tool. Figure 5 shows the schematic diagrams of the design; the size of comparator is small and also consumes low power due to the lesser number of transistors. The DC analysis of the TIQ comparator was performed. The DC analysis of the TIQ comparator output is shown in figure 6. This analysis shows different switching voltages of the comparator and these switching voltages are generated by changing the width of transistors.

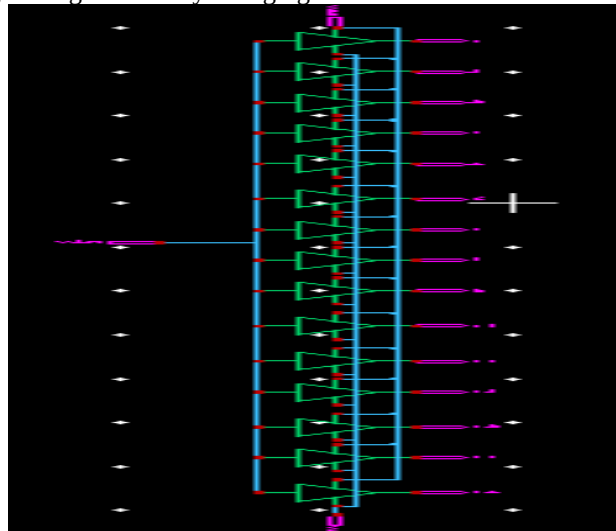


Figure 5. Schematic of TIQ comparator

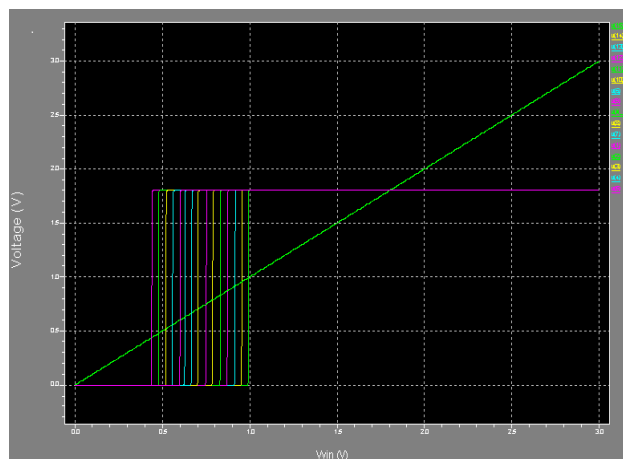


Figure 6. Different switching voltage of TIQ comparator

The careful selection of the values of W_n and W_p results in;

1. Reduced noise interference
2. Reduced overall power consumption of all the comparator

3. Reduced global cross talk delays
4. Minimize load capacitance

In the proposed design the analog input is successfully converted in to 15 bit digital output.

V. CONCLUSION

In proposed design the TIQ Comparator circuits are designed with different W_p and W_n values and simulated in tanner tool using 0.25 μm CMOS technology with 0.99V power supply. The static power consumption in TIQ comparator is found to be negligible and so the total power consumption is reduced to its minimum level thereby making this TIQ comparator acceptable for low power consumption and high speed flash ADC.

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