



International Journal of Emerging Technologies in Computational and Applied Sciences (IJETCAS)

www.iasir.net

SVL leakage current technique applied in 1-bit adder in VLSI

Shivam Singh Kushwah, Rupesh Maheshawari, Yogeshver Khandagare,
Department of Electronics & Communication,
Trinity Institute of Technology and Research,
Bhopal, M.P. India,

Abstract: very high processing power is one of the most important characteristics of any system and also portability is needed. This trend towards portable, distributed system architectures is one of the main dynamic forces for system integration, highly powerful systems such as those required for network computing (NC) and video services. In this research paper used a self controllable voltage level (SVL) technique to reduce a low leakage power. In implementation of SVL technique used a circuit of 1-bit adder. Adder basically perform the addition operation gives the result sum and carry. The simulation is done by using a microwind 3.1 and dsch 2 versions by using a 0.12 μ m technology. Used a design rule checker (DRC) for any implementation fault in the layout diagram. If circuit is design with some features like a low power, reliable performance, high speed and reduction of leakage current gives the benefits for the system. If we have used a self controllable voltage level technique in implementing we get these some parameter. The reduction of 67% of leakage current and 50% reduction of power dissipation by using SVL technique.

Keywords: SVL technique, low power, leakage power, High performance, high speed.

I. Introduction

Here logic circuit is first translated into a CMOS circuit and the initial layout is done. Once a full circuit depiction is obtain from the initial layout. Then the improved design will be implemented into a new layout and the design-analysis cycle will be repeated until all of the design specifications are met. For translating the gate-level design into a transistor-level circuit description. The sum out and the carryout functions are represented by nested AND-OR- NOR structures. Each such combined structure can be realized in CMOS as follows: the AND terms are implemented by series-connected nMOS transistors, and the OR terms are implemented by parallel-connected nMOS transistors. The input variables are applied to the gates of the nMOS and complementary pMOS transistors. Thus, the nMOS net may consist of nested series-parallel connections of nMOS transistors between the output node and the ground. The resulting transistor-level design of the CMOS 1-bit adder circuit. The circuit contains a total of 14 nMOS and 14 pMOS transistors, together with the two CMOS inverters which are used to generate the outputs. Initially, we will design all nMOS and pMOS transistors with a (W/L) ratio which is the minimum transistor size. The initial layout using minimum-size transistors is the 1-bit adder circuit is generated. One approach to increase switching speed, and thus, to reduce delay times, would be to increase the (W/L) ratios of all transistors in the circuit. However, increasing the transistor (W/L) ratios also increases the gate, source, and drains areas and as a result, increases the parasitic capacitances loading the logic gates. Hence, the resizing of transistors is firmly an iterative process which involves several cycles of successive layout modification, circuit extraction, and simulation.

II. History Of Work

Here we have discussed some research paper. A generalized topological optimization tool for array-based layout styles is presented in [1]. The paper presents a detailed study on the idle leakage reduction techniques on partially depleted silicon-on insulator (PD-SOI) CMOS SRAM [2]. In the VLSI-oriented fast, efficient, lossless image compression system (FELICS) algorithm is presented in this [3]. Multilevel design optimization approach for reducing the power dissipation of a pipelined analog-to-digital converter (ADC) have presented in [4]. Sleepy stack approach is used to reduce leakage power in [5]. CLB clustering design technique that employs VDD programmable and power gating methods to reduce leakage in standby mode in [6]. In Stack forced approach, decent leakage power reduction is achieved with large delay overhead, for all CMOS, CPL and TG logic style based circuits in this [7]. Technique to the Weibull distribution that extends delay and slew metrics for step inputs to the more general and realistic non-step inputs have presented in [8]. 8-bit 300MS/s 7-stages parallel pipeline ADC with 1.5-bit per stage and power efficient architecture is designed by sharing an amplifier

between two pipeline stages, introducing the proper clock timing between the two parallel stages describes in [9]. As technology scales down both VDD and Vt has to decrease to maintain historical delay reduction, while restraining active power dissipation in this [10]

III. Proposed Work

The proposed work is one-bit full adder circuit is one of the most widely used building blocks in all arithmetic (data processing) and digital signal processing architectures. In the following, we will examine the circuit structure and the realization of the full adder using the conventional CMOS design style. The sum-out and carry-out signals of the full adder are defined as the following two combinational Boolean functions of the three input variables, A, B, and C.

$$\begin{aligned}\text{sum_out} &= A \oplus B \oplus C \\ &= ABC + A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C \\ \text{carry_out} &= AB + AC + BC\end{aligned}$$

A gate-level realization of these two functions is shown in figure 1. Note that instead of realizing the two functions independently, we use the carry-out signal to generate the sum output. This implementation will ultimately reduce the circuit complexity and, hence, save chip area. Also, we identify two separate sub-networks consisting of several gates which will be utilized for the transistor-level realization of the full-adder circuit. The transistor-level design of the CMOS full-adder circuit is shown in Figure 2. The circuit contains a total of 14 nMOS and 14 pMOS transistors, together with the two CMOS inverters which are used to generate the outputs.

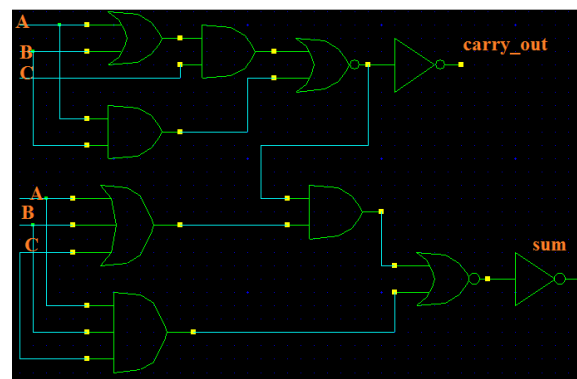


Figure 1 Gate-level schematic of the one-bit full-adder circuit

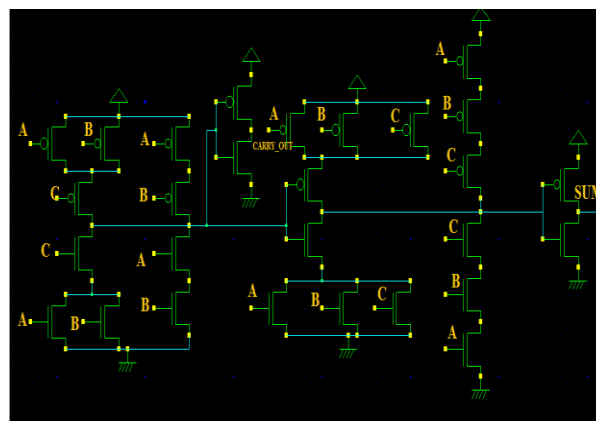


Figure 2 Transistor-level schematic of the one-bit full-adder circuit.

The layout of the full-adder circuit shown in figure 3 in which have designed using the simple layout optimization strategy. However, that all nMOS and pMOS transistors in this layout have the same (W/L) ratio.

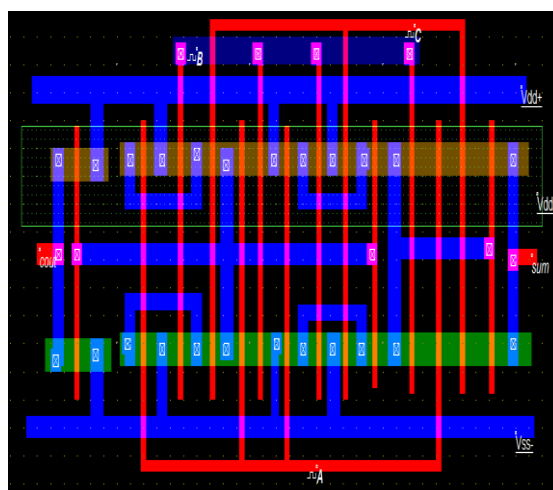


Figure 3 layout diagram of 1-bit adder

The waveform of voltage vs time shown in figure 4 in which carry is high only when the two or three high signal is added otherwise it is low and sum is high if any of three signal is high at a time. In figure 5 shows the voltage vs current waveform in which you can look that the leakage current is about 0.058ma and number of fluctuations is more.

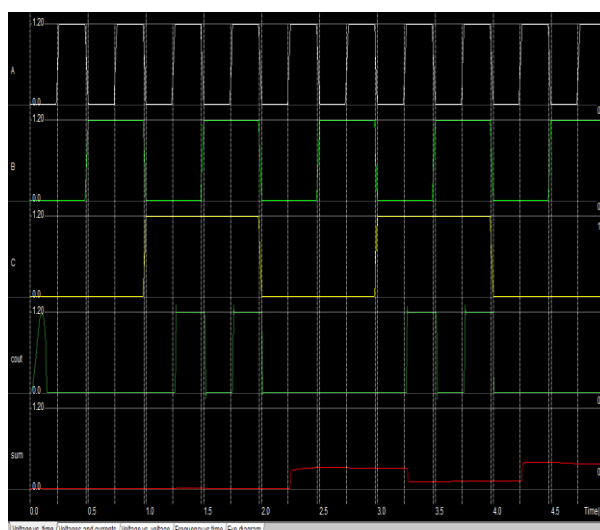


Figure 4 waveform of voltage vs time

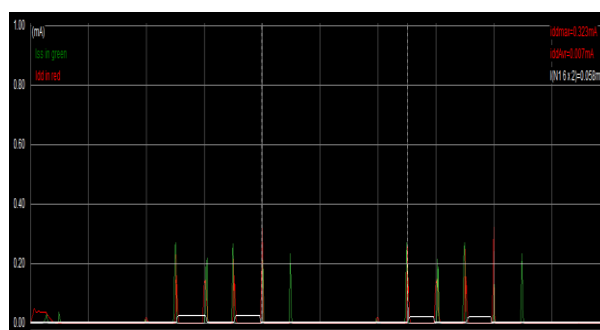


Figure 5 waveform of voltage vs. current

In figure 6 shows the layout diagram of 1-bit adder with self controllible voltage level (SVL) Technique in which used an extra circuitry for controlling the leakage current.

The SVL is divided into two parts: upper SVL and lower SVL. Upper SVL is connected to VDD and lower SVL is connected to ground. In upper and lower SVL used a one NMOS and PMOS and gate is connected together and apply a pre charge voltage of 1V.

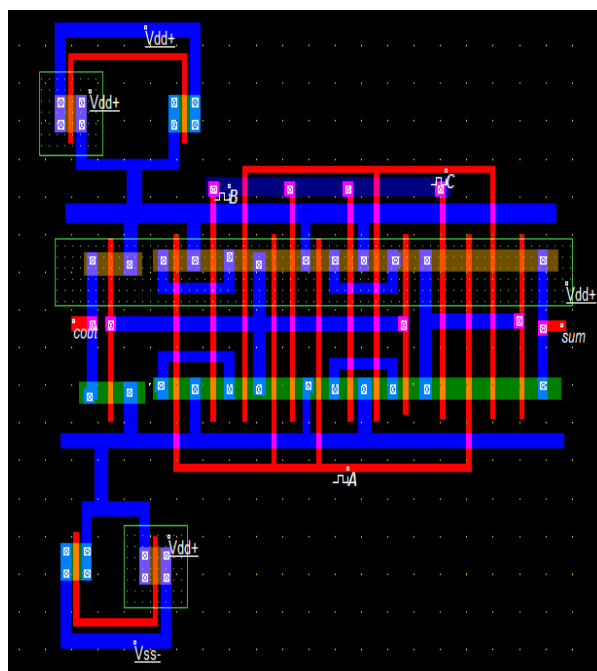


Figure 6 layout diagram of 1-bit adder with SVL Technique

Figure 7 shows the waveform of voltage vs. currents in which the leakage current is 0.022ma when implementing the self controllable voltage technique.

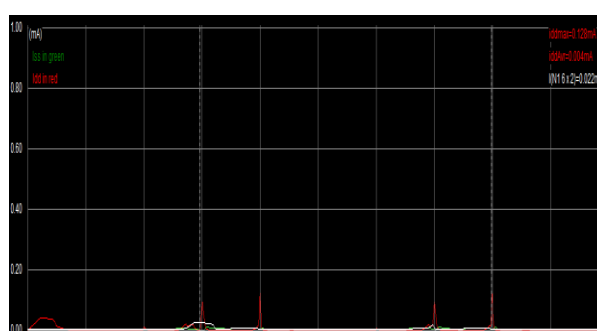


Figure 7 waveform of voltage vs. currents

IV. Circuit Simulation Result

The simulated input and output voltage waveforms of the one-bit CMOS full adder are represented above in number of figures. The 1-bit adder circuit presented here, which accepts 3 -bit binary numbers as input and produces the binary sum at the output and carry output. Simulation is done by using MICROWIND 3.1 and DSCH 2 in which used a 0.12 μ m technology. Simulation result of SVL based 1 Bit Adder in which leakage current is 0.058ma and with SVL technique leakage current is 0.022ma.

V. Conclusions

1-bit adder is simulated by using MICROWIND3.1 and DSCH2 software with 0.12 μ m technology. Here leakage current reduction technique is used in 1- bit adder. MICROWIND3.1 has a design rule checker, some generators and palette with 6 metals and 27°C temperature. By using a self controllable voltage technique to reduce the 67% of leakage current in 1-bit adder and 50% power consumption.

VI. References

1. Sriniv As Dev Adas A N D A. Richard Newton, Senior Member, IEEE, "Topological Optimization Of Multiple-Level Array Logic," IEEE Transactions On Computer-Aided Design. Vol Cad-6. No. 6. November 1987.
2. Olivier Thomas, Marc Belleville, Richard Ferrant, IEEE Member , "Sram Memory Cell Leakage Reduction Design Techniques In 65nm Low Power Pd-SOI CMOS," IEEE 2008.
3. Tsung-Han Tsai, Member, IEEE, Yu-Hsuan Lee, And Yu-Yu Lee," Design And Analysis Of High-Throughput Lossless Image Compression Engine Using VLSI-Oriented Felics Algorithm" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 18, No. 1, January 2010.
4. Jintae Kim, Member, IEEE, Sotirios Limotyrakis, Member, IEEE, And Chih-Kong Ken Yang, Senior Member, IEEE, "Multilevel Power Optimization Of Pipelined A/D Converters," IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 5, May 2011.
5. Jun Cheol Park And Vincent J. Mooney Iii, Senior Member, IEEE, "Sleepy Stack Leakage Reduction," IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 14, No. 11, November 2006.
6. Mohammad Mehdi Tohidi And Nasser Masoumi , "Fpga Leakage Power Reduction Using Clb-Clustering Technique," IEEE 2010.
7. Anup Jalan And Mamta Khosla , "Analysis Of Leakage Power Reduction Techniques In Digital Circuits," IEEE 2004.
8. Rajib Kar, Vikas Maheshwari, Sangeeta Mondal, Ashis K. Mal, A.K.Bhattacharjee "A Novel And Acurate Delay And Slew Metrics For Ramp Inputs For On-Chip VLSI Rc Interconnect Using Weibull Distribution Function", In Second International Conference On Computing, Communication And Networking Technologies 2010.
9. Manas Kumar Hati, Tarun K. Bhattacharyya , "A 55-Mw 300ms/S 8-Bit Cmos Parallel Pipeline Adc," 25th International Conference On VLSI Design 2012.
10. Rajendra Prasad S, B K Madhavi, K Lal Kishore, "Reduction Of Leakage-Power In Cntfet Sram Cell Using Stacked Sleep Technique At 32nm Technology," IEEE International Conference On Advances In Engineering, Science And Management (Lcaesm -2012) March 30, 31, 2012.