



International Journal of Emerging Technologies in Computational and Applied Sciences (IJETCAS)

www.iasir.net

Threshold Voltage Roll-Off Due to Channel Length Reduction for a Nanoscale n-channel FinFET

M. Zakir Hossain¹ and Quazi D. M. Khosru²

¹Department of Electrical and Electronic Engineering

Dhaka University of Engineering and Technology, Gazipur-1700, BANGLADESH

²Department of Electrical and Electronic Engineering

Bangladesh University of Engineering and Technology

Dhaka-1000, BANGLADESH

Abstract: As the device feature size enters into the nanoscale, the modeling and simulation of short channel effects in FinFETs devices become challenging. In this paper an easy approach to model short channel effects threshold voltage roll-off in nanoscale n-channel FinFETs is presented. The decrease of threshold voltage with decrease in gate length is a well-known short channel effect called the “threshold voltage roll-off” has been simulated. By using this threshold voltage, current-voltage characteristics have been observed for different operating regions of FinFETs with different channel lengths and also for different oxide thickness. In order to justify the validity of the proposed model the simulation results have been compared with the available experimental and/or simulation data. The analytical expressions derived in the present model can be a useful tool in device design and optimization.

Keywords: Nanoscale FinFET, Short-Channel Effects (SCE), threshold voltage roll-off, inversion carrier, effective mobility.

I. Introduction

FinFETs are the most promising device structures to address short channel effects and leakage issues in deeply scaled CMOS. As the dimensions of MOS devices are shrunk, the close proximity between the source and drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the “short-channel effects” start plaguing. Calculation of threshold voltage, which is a fundamental parameter in device characterization and modeling [1], is an important step towards having an in depth understanding of the electrostatics and dynamic behavior of this novel device. The FinFET characteristics in previous models [2]-[4] were not described in terms of threshold voltage roll off. A physics based model is studied [4] using semi-classical 3D Monte Carlo device simulator to investigate important issues in the operation of FinFETs. Fast Multipole Method (FMM) has been integrated with the EMC (Ensemble Monte Carlo) scheme to replace the time consuming Poisson equation solver. Effect of unintentional doping for different device dimensions has been investigated and the result shows that the effect of unintentional doping becomes dominant near sub-threshold regime where number of mobile carriers is very few. Moreover, threshold voltage and DIBL in terms of body doping for nanoscale SOI FinFET is studied and compared with Bulk FinFET [5]. The quantum definition based threshold voltage is evaluated for triple-gate (TG) SOI FinFETs using self consistent Schrödinger-Poisson solver [6]. However, short channel threshold voltage roll-off is missing in literature.

In addition, a self-consistent solution of time consuming 3D Poisson-Schrödinger equation is obtained using multiresolution approach to estimate potential profile, subthreshold swing and threshold voltage roll-off [7]. Furthermore, threshold voltage roll-off is observed [8] for short channel FinFET devices, without the detailed analysis of how this method of calculating threshold voltage roll off can be applicable for a wide range of device family.

In this paper, a self-consistent method as an easy approach to model short channel threshold voltage roll-off in nanoscale SOI n-channel FinFETs has been proposed. Threshold voltage has been simulated with respect to work function and the physical device parameters. Then threshold voltage shift has been observed due to different channel length and oxide thickness. By using this threshold voltage, current-voltage characteristics have been simulated for different operating regions of FinFETs of different channel lengths. For suitable arrangement, the rest of the paper is organized as: section II describes the proposed threshold voltage roll-off methodology and device parameters. In Section III, the results of the model of the FinFETs devices are

presented with an insight to their physical meaning. Section IV concludes the paper.

II. Simulation Model

Due to their excellent control over short channel effects and their superior current driving ability, FinFETs have been regarded as a promising replacement for the conventional bulk CMOS [9]. The structure of a FinFET is shown in Fig.1. Even though current conduction is in the plane of the wafer, it is not strictly a planar device. Rather, it is referred to as a quasi-planar device, because its geometry in the vertical direction (viz. the fin height) also affects device behavior. The gate wraps around the body from three sides, and this is responsible for higher gate-channel control and therefore reduced SCE. The calculation of threshold voltage for FinFET devices is based on the method shown in [10], where 2D charge profile is calculated along the cross section perpendicular to the transport direction (Fig. 1).

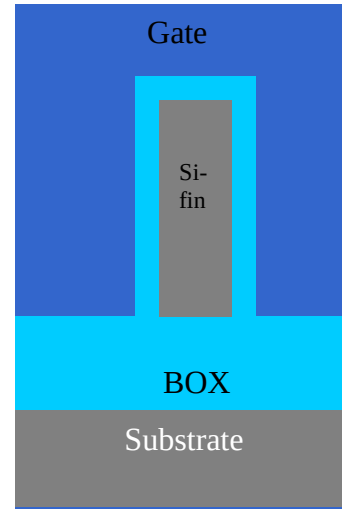


Fig.1. Test device of an n-Channel FinFET (2D cross-section along transistor gate (SOI)).

For multigate MOSFET the relation between the physical device parameter and threshold voltage is given as [11]:

$$V_{th} = \phi_{ms} + \frac{kT}{q} \ln \left(\frac{2C_{ox}kT}{q^2 n_i t_{si}} \right) + \frac{h^2 \pi^2}{2m t_{si}^2} \quad (1)$$

The first term of (1), is the work function difference between the gate and the silicon film, which is equal to -0.17eV in our simulations. The second term represents the potential Φ in the channel; it is inversely proportional to the silicon film thickness t_{si} and also depends on the oxide thickness. The third term is the lowest subband energy above conduction band minima. It is a quantum mechanical term which varies depending on the splitting of the conduction band energy level into subbands. The value of this is taken from the literature [10] for double gate FinFET.

The decrease of threshold voltage with decrease in gate length is a well-known short channel effect called the “threshold voltage roll-off”. As the channel of the device is reduced to nanoscale region, the charge distribution in the channel is influenced by the field originating from the source/drain. The critical geometry parameters which determine device short-channel behaviors spatially threshold voltage roll-off are gate length, fin thickness, fin height, oxide thickness and channel doping [11].

Threshold voltage fluctuation for channel length reduction can be found by the following expression [12]:

$$\Delta V_{th} = -\frac{qN_a W_m r_j}{C_{ox} L_{ch}} \left[\sqrt{1 + \frac{2W_m}{r_j}} - 1 \right] \quad (2)$$

Where r_j is the depth of the source and drain junction, W_m the maximum width of the depletion layer, L_{ch} is the device channel length. The values of different parameters are available in [9]. Threshold voltage roll-off can be found by subtracting ΔV_{th} from the threshold voltage, V_{th} as:

$$\text{Threshold voltage roll-off} = V_{th} - \Delta V_{th} \quad (3)$$

Moreover, semi-classical expressions are used for I-V characteristics [13].

The channel conductance of the device also depends on threshold voltage, is defined by the following expression [14]:

$$g_d = \frac{W_{eff} \mu_{eff} C_{ox}}{L_{ch}} (V_{gs} - V_{th}) \quad (4)$$

where W_{eff} is the channel width or effective channel width and μ_{eff} the effective mobility. The MOSFET transconductance is defined as the change in drain current with respect to the corresponding change in gate voltage. The transconductance for an n-channel device operating in the linear region is given as [12]:

$$g_m = \frac{W_{eff} \mu_{eff} C_{ox}}{L_{ch}} V_{ds} \quad (5)$$

The transconductance for the saturation region can be found as [12]:

$$g_m = \frac{W_{eff} \mu_{eff} C_{ox}}{L_{ch}} (V_{gs} - V_{th}) \quad (6)$$

III. Result and Discussion

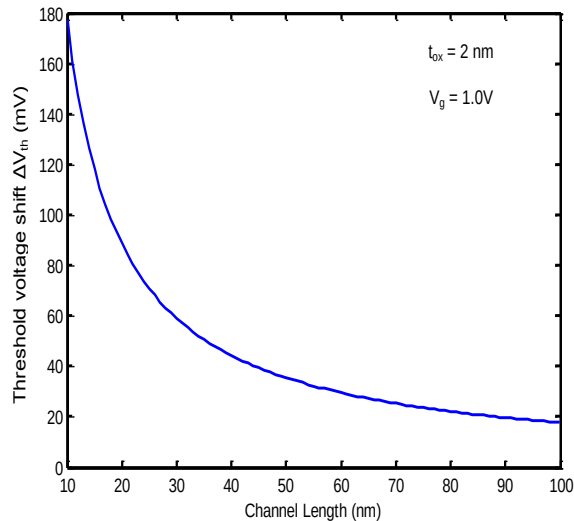


Fig.2: Threshold voltage shift (ΔV_{th}) with channel length.

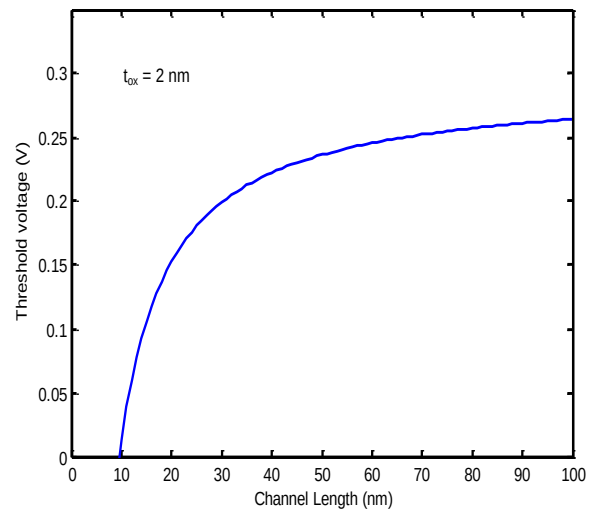


Fig.3: Threshold voltage roll-off for nanoscale FinFET.

Threshold voltage shift with respect to channel length is shown in Fig.2. It is seen that threshold changes sharply above channel length of 60 nm, after this the fluctuation of threshold voltage is comparatively less. Threshold voltage changes due to the reduction of charges in the depletion layer for reduction of channel length. From the Eq.(2), threshold voltage roll-off also depends on oxide layer substrate impurity doping concentration (N_a). As the thickness of oxide is decreased, less gate voltage is required for strong inversion. Threshold voltage roll-off is shown in Fig.3. For shorter channel lengths, the value of threshold voltage reduces.

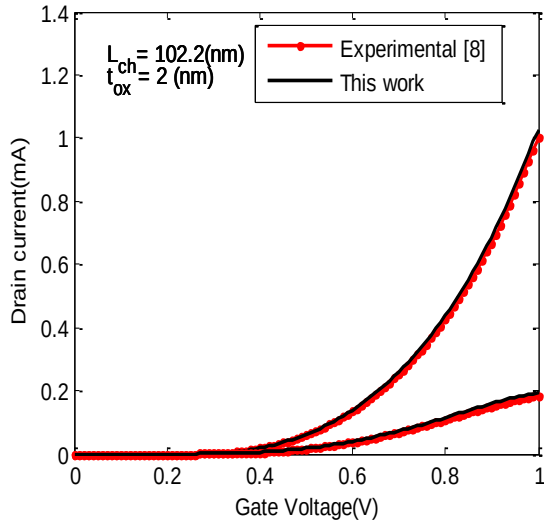


Fig.4: Drain current versus gate voltage.

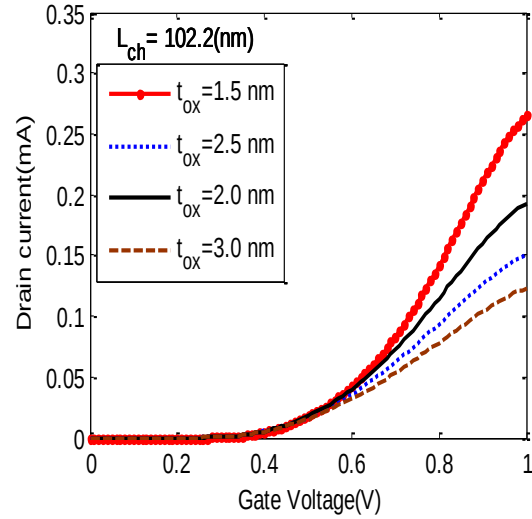


Fig.5: Effect of oxide thickness on drain current.

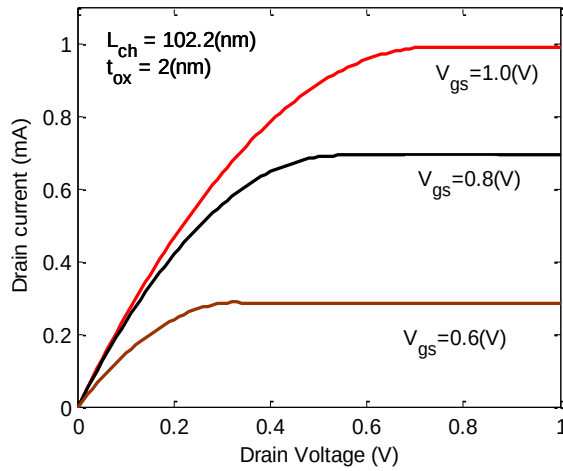


Fig.6: Drain current versus drain voltage.

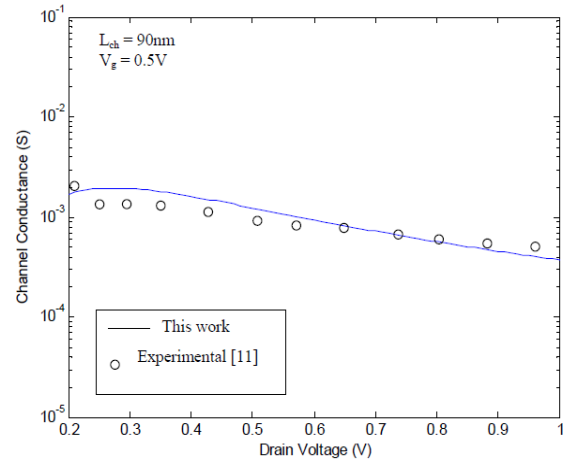


Fig.7: Channel conductance versus drain voltage.

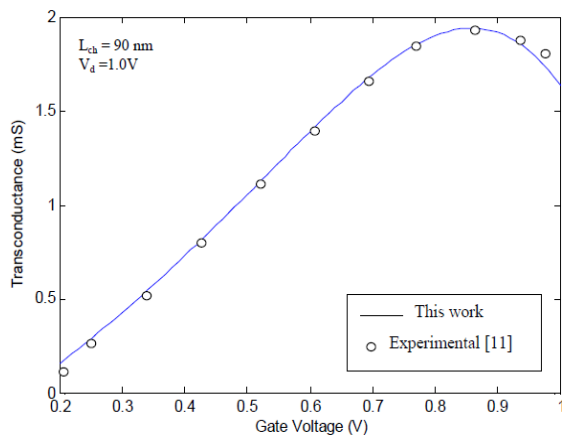


Fig.8: Transconductance versus gate voltage.

The drain current versus gate voltage is shown in Fig.4. The continuous lines for this work and the circles represent the experimental results. Drain current are plotted for 50mV and 1.0V of drain voltages and compared with the experimental data. It is seen that the transfer characteristics lies very close to the experimental results

for low as well as high drain bias. The effect of oxide thickness on drain current versus gate voltage is plotted in Fig.5. It is seen that when the oxide thickness is increased, the drain current decreases and the curves move downward. This is because, the oxide capacitance increases with the decrease in oxide thickness and the oxide capacitance is directly proportional to the drain current.

The drain current versus drain voltage of channel length 102.2 nm FinFET with oxide thickness 2 nm is plotted in Fig.6. The effect of gate voltage on the output characteristics has also observed. It is seen that as the gate voltage is decreased, the drain current curves move downward. The saturation current increases at higher gate bias.

The channel conductance or output conductance is observed with respect to drain voltage is shown in Fig.7 in semi log scale for channel length of 90 nm. The other dimensions of this device are available in the literature [11]. When gate voltage, V_{gs} is larger than V_{th} , channel inversion charge density increases, which increases the channel conductance. At saturation, the increment of channel conductance at the drain becomes zero, which means that the slope of I_D versus V_D curve is zero and hence at this region conductance remain constant. The transconductance of n-channel FinFET of channel length 90 nm versus gate voltage is plotted in Fig.8. Here the drain voltage is kept constant for both the linear and saturation regions in order to observe the effect of effective mobility. As the effective mobility increases linearly with the increase in gate voltage, transconductance also increases. At higher value of gate voltage, effective mobility decreases hence transconductance also decreases.

IV. Conclusion

This paper shows a simple approach of threshold voltage roll-off methodology for nanoscale n-channel FinFET. The mathematical expression for threshold voltage roll-off has developed. By using this expression the threshold voltage roll-off has been simulated by considering the different physical device parameters and device channel length. Moreover, transfer characteristics and output characteristics of the device for channel length 102.2 nm and oxide thickness 2.0 nm have observed. The results show a very good agreement with the experimental data. Furthermore device channel conductance and transconductance have been simulated and compared with experimental results. The effect of oxide thickness on I-V characteristics has also been simulated and shows that it has a great impact on drain current. To further development of this model, other realistic effects can be accounted, such as 3D parasitic effects that are especially severe in FinFETs.

References

- [1] A. Ortiz-Conde, F. J. Garcia Sanchez, J. J. Liou, A. Cerdeira, M. Estrada, Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectronics Reliability*, vol. 42, no. 4-5, pp. 583-596, Apr.- May 2002.
- [2] D.S.Woo, J.H.Lee, W.Y.Choi, B.Y.Choi, Y.J.Choi, J.D.Lee, B.G.Park "Electrical Characteristics of FinFET with vertically nonuniform source/drain doping profile." *IEEE Trans. on Nanotechnology*, vol.1, no.4, Dec. 2002.
- [3] G. Kathawala, M. Mohamed and U.Ravaioli, "Comparison of Double-Gate MOSFETs and FinFETs with Monte Carlo Simulation", *Journal of Computational Electronics* 2: 85–89, 2003.
- [4] H. R. KHAN, D. VASILESKA and S. S. AHMED, "Modeling of FinFET: 3D MC Simulation Using FMM and Unintentional Doping Effects on Device Operation", *Journal of Computational Electronics* 3: pp. 337–340, 2004.
- [5] M. Poljak, V. Jovanovic, T.Suligoj, "SOI Vs. Bulk FinFET: Body doping and corner effects influence on device characteristics". *Electrotechnical Conference*, 2008. MELECON 2008, pp. 425-430.
- [6] Md Emran Amin, Md. Zunaid Baten, Raisul Islam and Quazi D. M. Khosru, "Quantum Mechanical Effect on Determining Threshold Voltage of Trigate FinFET Using Self- Consistent Analysis", *TENCON 2009, IEEE Region 10 Conference* (2009).
- [7] R. Ramesh, M. Madheswaran, K. Kannan, "Self-consistent 3-D numerical modeling of a uniformly doped nanoscale FinFET using interpolating wavelets", *J Comput Electron* (2011) 10:331–340, Springer.
- [8] J. Song, Y. Yaun, B. Yu, W. Xiong and Y. Taur, "Compact modeling of experimental n- and p-channel FinFETs", *IEEE Trans. on Electron Devices*, vol.57, no.6, June. 2010.
- [9] J. Song, B. Yu, W. Xiong, and Y. Taur, "Gate-Length-Dependent Strain Effect in n- and p-Channel FinFETs", *IEEE Trans. on Electron Devices*, vol.56, no.3, March 2009.
- [10] Se Re Na Yun, Chong Gun Yu, Jong Tae Park, Chi Woo Lee, D. Lederer, A. Afzalian, Ran Yan, J.P. Colinge, "A quantum definition of threshold voltage in MuGFETs," in *IEEE International SOI Conference Proceedings*, 2007.
- [11] J.-P. Codrings, "Multiple-gate SOI MOSFETs." *Solid State Electron*, vol.48, 6, pp.897-905, Jun. 2004.
- [12] Donald A. Neamen, "Semiconductor physics and devices: basic principles".
- [13] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain-current model for DG MOSFETs", *IEEE Trans. on Electron Devices letters*, vol.25, no.2, Feb. 2004.
- [14] S. M. Sze, "Physics of Semiconductor Devices", 2nd Edition.