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Design of Low Power 8 bit GDI Magnitude Comparator

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Abstract: Low power 8 bit GDI magnitude comparator is proposed in this paper which has an advantage of minimum power dissipation, reduced propagation delay and less number of transistors required as compare to conventional CMOS magnitude comparator. Proposed GDI magnitude comparator is designed at 100MHz frequency with 1.8 v supply voltage using 180nm technology using CADENCE VLSI EDA tools. The performance analysis of proposed GDI magnitude comparator is also compared with conventional CMOS comparator, Transmission Gate Comparator and NMOS Pass Gate Comparator. Simulation of all designs have been done using SPECTRE VIRTUOSO ADE tool and the results shows that proposed GDI magnitude comparator dissipate 72.55% less power, 22.52% less propagation delay and required 65.72% less number of transistors as compare to basic CMOS magnitude comparator.

Keywords: GDI magnitude comparator; Gate Diffusion Input technique; Low power VLSI design; twin-well technology; Silicon on Insulator.

I. Introduction

In the last twenty years or so by far, the strongest growth area of the semiconductor industry has been in silicon Very –Large Scale Integration (VLSI) technology. The sustained growth in VLSI technology is fuelled by the continued shrinking of transistors to ever smaller dimensions. The benefits of miniaturization are higher packing densities, higher circuit speeds, and lower power dissipation have been key in the evolutionary progress leading today's computers and communication systems that offer superior performance, dramatically reduced cost per function, and much reduced physical size, in comparison with their predecessors. VLSI circuits have found a lot of applications in the recent development of ICs. The dimensions of transistors have shrunk enormously, which has a great positive impact on VLSI technology. The evolution of VLSI device technology from the invention of first bipolar transistor, MOSFET, CMOS up to the VLSI era, the power dissipation aspects of various types transistor technology is always a researcher's interest. The CMOS circuits include both p-channel and n-channel MOSFET's which causes only negligible standby power dissipation. The active power dissipation occurring during switching activities can be minimized by good design of the circuits. By this characteristic, hundreds of millions of CMOS transistors can be integrated on a single chip. Also, the noise margin of CMOS-based circuits is improved leading to easy design of CMOS chip. The speed of silicon-based devices increased and cost decreased with the smaller sized ICs. The reduced feature size of silicon ICs rapidly increases the integration density [1]. Applications powered by a battery- pocket calculators, hearing aids, implantable pacemakers, portable military equipment used by individual soldier and most importantly, wrist watches – drove low power electronics. In all such applications, it is important to prolong the battery life as much as possible. And now with growing trend towards portable computing and wireless communication, power dissipation has become one of the most critical factors in the continued development of the microelectronics technology [2].

Power dissipation in CMOS can be classified into three categories: static power dissipation, dc switching power occurring when both transistors conduct momentarily during a transition, and ac switching power lost while charging (discharging) capacitive loads. The combination of dc switching power and ac switching power is often called dynamic power dissipation [3]. The power dissipation attributable to the three sources can be influenced at different levels of the overall design process. Minimization of power dissipation in CMOS based system designs can take place at four levels: technology, circuit, architecture and algorithm. At the circuit level, considerable potential for power saving exist by the proper choice of logic style for implementing combinational circuits. The various methodologies and topologies to achieve the required function such as conventional CMOS, nMOS Pass transistor logic and transmission gates can reduce layout area and consequently power dissipation [4]. nMOS Pass transistor logic technique is better than the conventional CMOS technique in high speed and low power logic circuit design because of reduced number of transistors. However, the major drawback of nMOS Pass transistor logic technique is the reduced drive current and hence slower speed of operation at the reduced supply voltage. A new logic style first proposed by A.Morgenshtein [5], GDI technique is superior over other design techniques in terms of low power and high speed VLSI design as this technique uses a simple GDI cell consisting of only two transistors, to implement various complex logic functions. This technique improves the logic level swing,

characteristic performances and also allows a simple design of any logic circuit using a small GDI cell. GDI technique enables simpler gates, lower transistor count, and lower power dissipation in many implementations, as compared with conventional CMOS, nMOS Pass transistor logic and transmission gates [5].

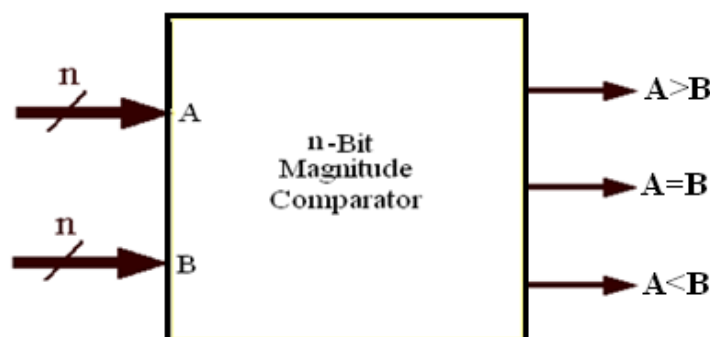
In digital system the magnitude comparator is a very useful and basic arithmetic component. A compact, good cost benefit, high-performance magnitude comparator plays an important role in almost all hardware sorters. One of the most important problems in computer science is sorting. Many fundamental processes in communication and computing systems require data sorting. Sorting network using comparator play a key role in the areas of parallel computing, multiprocessing and multi-access memories. A magnitude comparator is also used in microprocessor for decoding instructions and data processing in Digital Signal Processors (DSP). Advancement in the next generation communication systems also requires efficient digital comparators.

In this paper, GDI Magnitude Comparator is proposed which has an advantage of minimum power dissipation, reduced propagation delay and less number of transistors required as compare to conventional CMOS magnitude comparator. The paper is organized section wise. Section II presents the design procedure and architecture for Magnitude Comparator. Section III presents the design methodology of proposed GDI Magnitude Comparator. Section IV presents performance analysis of proposed 8 bit GDI Magnitude Comparator and its comparison with other conventional CMOS comparators. Section V concludes the paper with some remarks and thoughts for future work.

II. Algorithm for the design of Magnitude Comparator

A magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. An n bit magnitude comparator block [6] is shown in Fig. 1 and it compares two n bit binary numbers A and B and the outcome of the comparison is specified by three binary variable that indicates :: GT ($A > B$), EQ ($A = B$) and LT ($A < B$).

Figure 1 N bit magnitude comparator block



The circuit for comparing two n -bit numbers has 2^{2n} entries in the truth table and becomes too cumbersome even with $n=3$. Here an algorithm will derive for the design of a 4-bit magnitude comparator.

The algorithm is a direct application of the procedure a designer uses to compare the relative magnitudes of two numbers. Consider two binary numbers, A and B with 4 bits each. The coefficients of the numbers with descending significant are as follows:

$$A = A_3A_2A_1A_0$$

$$B = B_3B_2B_1B_0$$

The two numbers are equal if all pairs of significant bits are equal i.e., $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$, and $A_0 = B_0$. For the binary numbers, the bit values are either 1 or 0 and the equality relation of each pair of binary bits can be expressed logically with an equivalence function:

$$X_i = A_i B_i + A'_i B'_i \quad \text{where } i = 0, 1, 2, 3.$$

Where $X_i = 1$ only if the pair of bits in position i are equal, i.e., if both are 1's or both are 0's.

The equality of the two numbers, A and B , is displayed in a combinational circuit by an output binary variable which is designate by symbol EQ ($A = B$). This binary variable is equal to 1 if the input numbers, A and B , are equal, and it is equal to 0 otherwise. For the equality condition to exist, all X_i variables must be equal to 1. This dictates an AND operation of all variables:

$$(A=B) = X_3X_2X_1X_0 \quad \text{----- (1)}$$

The binary variable EQ ($A = B$) is equal to 1 only if all pairs of digits of the two numbers are equal.

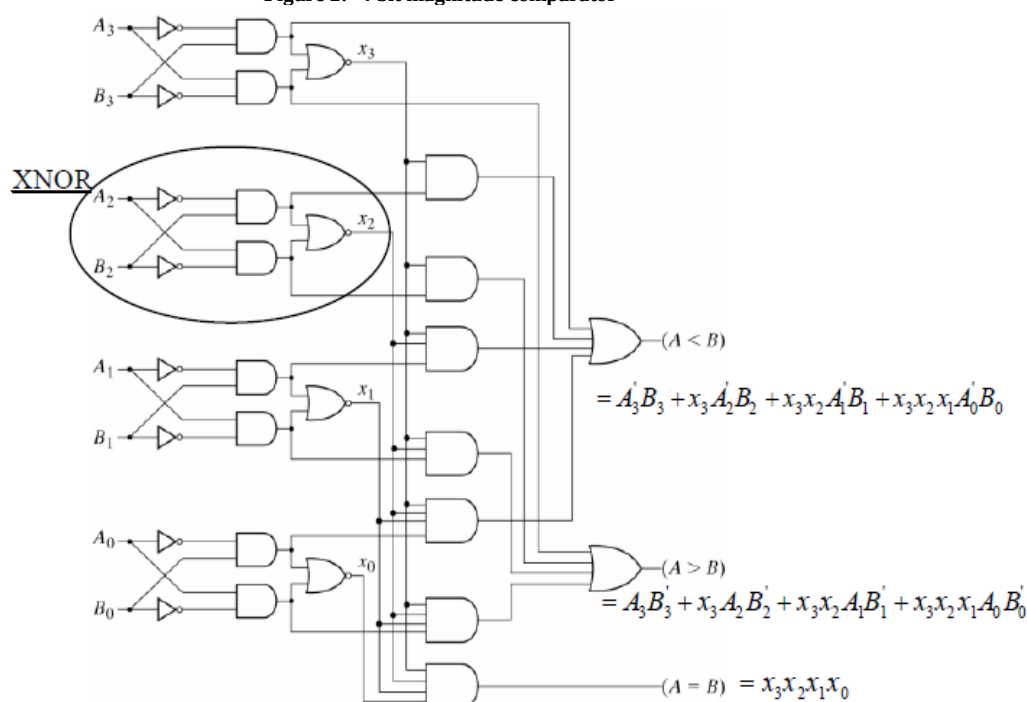
To determine if A is greater than or less than B , inspect the relative magnitudes of pairs of significant bits starting from the most significant bit position. If two bits are equal, then compare the next lower significant pair of bits. This comparison continues until a pair of unequal bits is reached. If the corresponding bit of A is 1 and that of B is 0, it concludes that $A > B$. also if the corresponding bit of A is 0 and that of B is 1, it concludes that $A < B$. the sequential comparison can be expressed logically by the following two Boolean functions:

$$GT(A > B) = A_3B'_3 + X_3A_2B'_2 + X_3X_2A_1B'_1 + X_3X_2X_1A_0B'_0 \quad \text{----- (2)}$$

$$LT (A < B) = A'_3 B_3 + X_3 A'_2 B_2 + X_3 X_2 A'_1 B_1 + X_3 X_2 X_1 A'_0 B_0 \quad \text{-----}(3)$$

The symbols GT ($A > B$) and LT ($A < B$) are binary output variables which are equal to 1 when $A > B$ or $A < B$, respectively.

Figure 2: 4 bit magnitude comparator



The gate implementation of the three output variables derived above is simple as it involves certain amount of repetition. The “unequal” outputs can use the same gates that are needed to generate the “equal” output. The logic diagram of the 4-bit magnitude comparator is shown in figure 2. The four X outputs are generated with equivalence (EX-NOR) circuits and applied to an AND gate to give the output binary variable ($A=B$). The other outputs use the X variables to generate the Boolean functions expressed in equation 2 and 3. This is a multilevel implementation and it has a regular pattern. We can follow the same procedure to obtain a magnitude comparator circuit for binary numbers with more than four bits.

In this paper same algorithm is used to design 8 bit magnitude comparator. To reduce power dissipation at the circuit level, different logic style such as CMOS, transmission gate (TG) and pass transistor logic (PTL) have been used to design combinational circuit. Each logic style has its own merits and demerits in terms of power dissipation, propagation delay, power delay product, area and output driving capability. Basically, CMOS fulfills all the requirements for ease-of-use of logic gates. On the other hand due to irregular transistor arrangements and high wiring requirements layout of pass-transistor cells is not as efficient and straightforward [8]. Some of the main advantages of PTL over standard CMOS design are high speed, due to the small node capacitances; low power dissipation, as a result of the reduced number of transistors; and lower interconnection effects, due to a small area. However, most of the PTL implementations have two basic problems. First, the threshold drop across the single-channel pass transistors results in reduced current drive and hence slower operation at reduced supply voltages; Second, since the “high” input voltage level at the regenerative inverters is not , the PMOS device in the inverter is not fully turned off, and hence direct-path static power dissipation could be significant [5].

In this paper proposed GDI magnitude comparator that allows solving most of the problems occurs in CMOS magnitude comparator and PTL magnitude comparator mentioned above. Here GDI stands gate diffusion input (GDI) technique. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library.

III. Design Methodology of proposed GDI Magnitude Comparator

Proposed GDI magnitude comparator is designed as per the algorithm explained in section II but the basic gates such as AND, OR, NOT and NOR are designed using GDI technique. A basic cell of GDI is shown in figure 3 contains four terminals. N, P and G are the input terminals while D is used as the output terminal. The bulk of nMOS transistor is connected to the bulk of pMOS transistor. Table 1 shows implementation of various logic

functions using single GDI cell. All the functions of table 1 can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies [5].

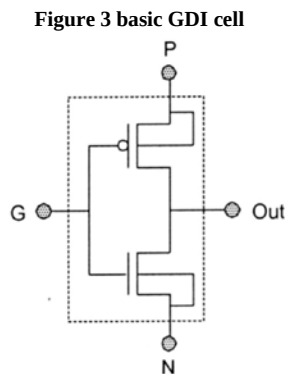


Table 1 Various Logic Functions of GDI Cell

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A} + B$	F2
'1'	B	A	$A + B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B + AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

The GDI cell allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors as compared to CMOS and existing pass transistor logic techniques, while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library. A simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard pass transistor logic (PTL) implementations, but very simple (only two transistors per function) in the GDI design method. Figure 4 shows the implementations of AND, OR and NOR gates in GDI which are the basic gates in magnitude comparator.

Figure 4 Implementations of AND, OR and NOR gates in GDI cell

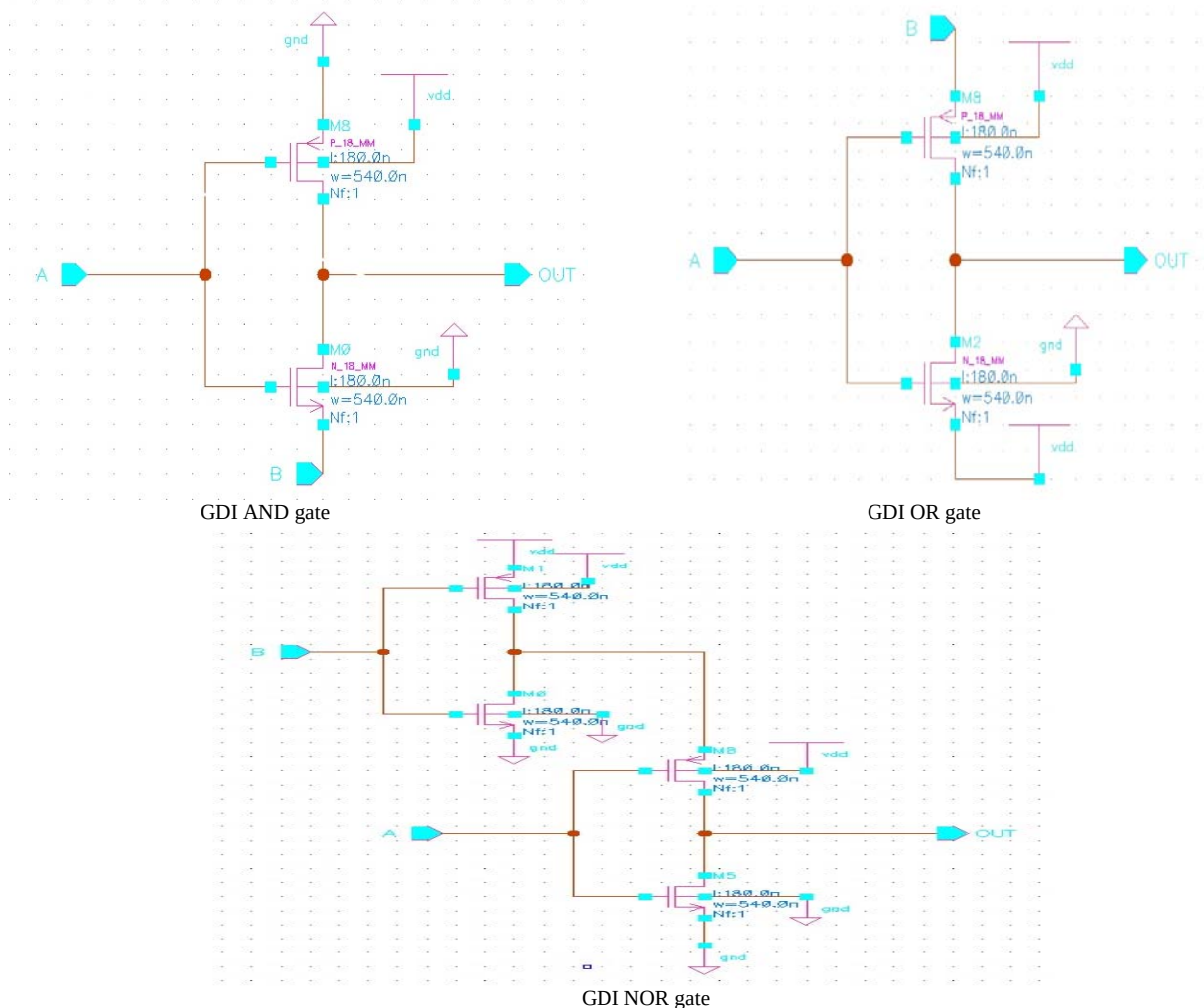


Table 2 Performance Analysis of AND, OR, NOR using GDI, CMOS, TG and NPG technique

Logic style	AND gate			OR gate			NOR gate		
	Power (μ W)	Delay (nsec)	No. of Transistors	Power (μ W)	Delay (nsec)	No. of Transistors	Power (μ W)	Delay (nsec)	No. of Transistors
GDI	0.149	10.05	2	0.123	20.05	2	1.314	19.93	4
CMOS	1.459	10.05	6	2.307	20	6	1.119	19.99	4
TG	1.904	10.09	6	2.887	20.04	6	3.873	4.946	8
NPG	1.472	10.07	4	1.727	20.06	4	2.94	19.99	6

The GDI cell has $n+2$ inputs when compared to CMOS. In [5] the performance of GDI was analyzed in terms of noise margin, body effect, fan out, delay etc. In realizing the function $F1 = A'B$, it has been found that the behavior of GDI cell is similar to that PMOS pass transistor logic in which the output will be V_{tp} instead of 0. This is the only case where logic degradation of one V_t takes place. To restore the logic, buffer can be added at the output. GDI cell can act as a buffer when $B = 1$ which also performs its logic evaluation. This is a main advantage. With proper connection of the cells, several GDI cells can be connected without accumulating the voltage drop. In order to restore the swing an output inverter can be used which can also perform its logical function. In this way, the V_t drop and noise margin reduction are localized [5] [9].

However, there are also potential advantages in GDI in terms of reliability: - 1) The lower voltage levels may have lower impact due to crosstalk on neighboring wires. 2) The fact that complex functions can be built by using multiple instances of the same GDI cell may contribute to reduced variability. 3) Smaller area and number of transistors in GDI means shorter interconnects and thus less crosstalk, and enable more efficient place and route. Figure 5 shows block diagram of proposed GDI magnitude comparator.

IV. Simulation results and Performance Analysis

In our research we designed 4 and 8 bit magnitude comparator based on GDI technique. Its performance is analyzed and compared with CMOS, TG and NPG techniques. Schematic design of comparator is done using CADENCE VLSI EDA tool using 180nm technology. In our designed we used both pMOS and nMOS transistor of width = 540nm and length= 180nm. Schematic designed is simulated at 1.8v with 100MHz frequency using SPECTRE VIRTUOSO simulator of CADENCE. In our design, we used AND, OR gate instead of NOR gate as GDI NOR gate consumes little more power compared to CMOS NOR gate, refer table 2. We examined our circuit for three different inputs $A=11111111$, $B=11111111$; $A=01111111$, $B=11111111$ and $A=10000000$, $B=01111111$. The schematic circuit design of proposed GDI Magnitude Comparator and its output power waveform are shown in figure 6 and 7 respectively.

Figure 6: Circuit design of proposed GDI Magnitude Comparator

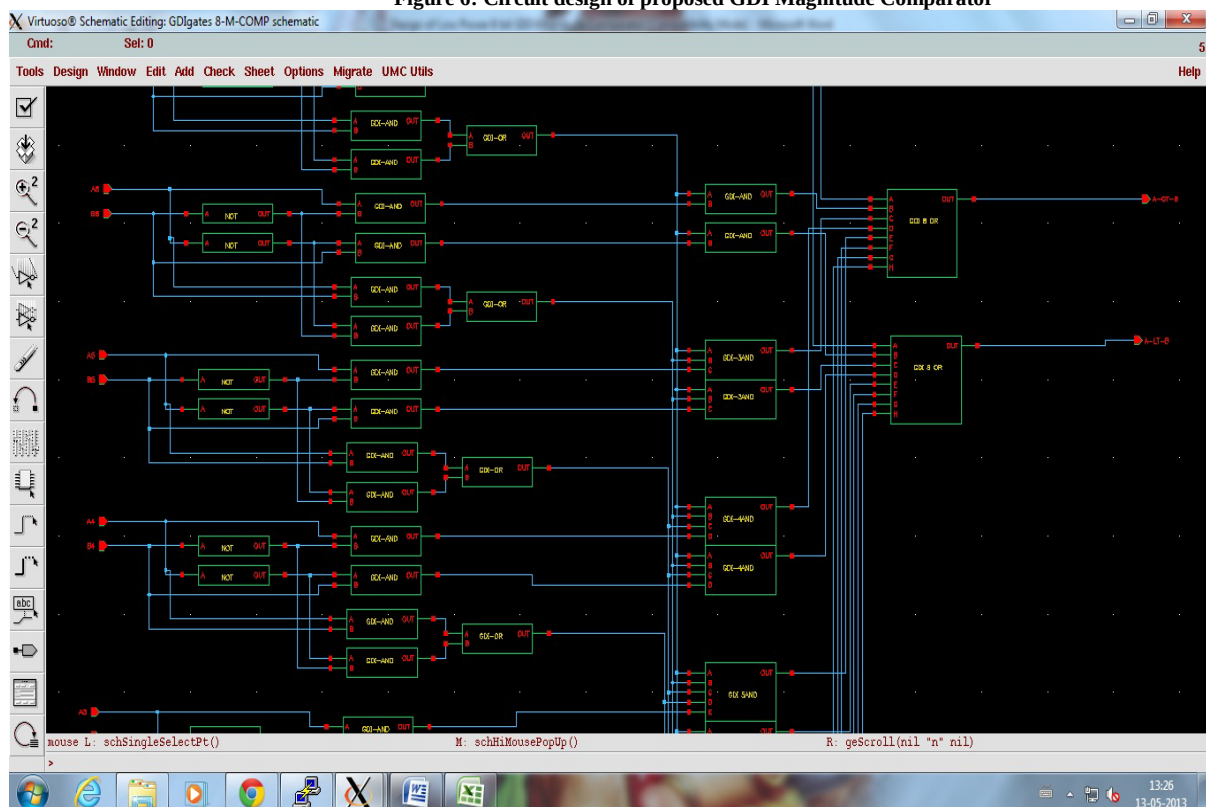
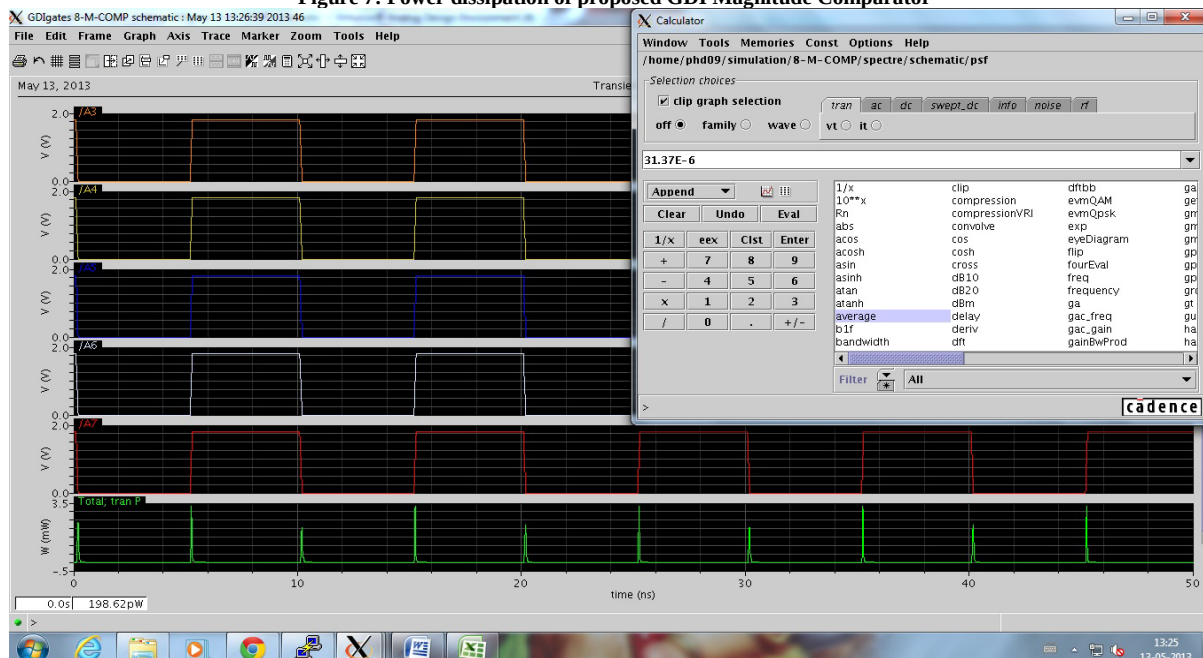


Figure 7: Power dissipation of proposed GDI Magnitude Comparator

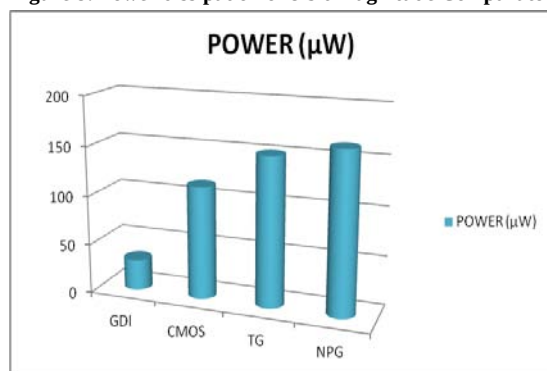
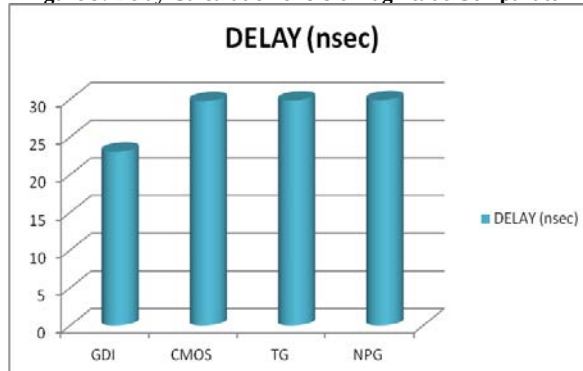
Different input combinations are applied at the input of comparator and analyzed for greater than, less than and equal to values. Performance and comparative analysis of 4 and 8 bit magnitude comparator using different logic style are shown in table 3. The GDI based 4bit comparator dissipates $9.864 \mu\text{W}$ power and has a delay of 20.47 nanosecond where as CMOS comparator dissipate $53.2 \mu\text{W}$ power and 25.46 nanosecond propagation delay. For 8 bit comparator, GDI dissipates $31.37 \mu\text{W}$ power which is almost 72.55% less than CMOS comparator. Also GDI based comparator is faster than other techniques and it uses less area.

Table 3: Performance and Comparative analysis of different 4 and 8 bit magnitude comparator

Logic style	4 bit magnitude comparator			8 bit magnitude comparator		
	Power (μW)	Delay (nsec)	Area (μm^2)	Power (μW)	Delay (nsec)	Area (μm^2)
GDI	9.864	20.47	10.108	31.37	23.05	25.8552
CMOS	53.2	25.46	27.216	114.3	29.75	75.4272
TG	66.22	25.45	27.216	150.9	29.84	75.4272
NPG	177.8	25.5	27.216	163.2	29.89	75.4272

V. Conclusion

The comparative performance of 8 bit magnitude comparator is also shown by graph for power and delay calculation. From the figure 8 & 9, we conclude that magnitude comparator based on GDI technique dissipate 72.55% less power , 22,52% less propagation delay and it needs 65.72% less area as compare to basic CMOS magnitude comparator. As the number of transistors used in AND, OR gate in CMOS, TG and NPG technique are same, the area of designing comparator using these logic styles are same. Among the presented design techniques, GDI proves to have the best performance values and lowest transistor count.

Figure 8: Power dissipation of 8 bit Magnitude Comparator**Figure 9: Delay Calculation of 8 bit Magnitude Comparator**

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