



## **4T DRAM based on Self-controllable Voltage Level technique for low leakage power in VLSI**

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**Abstract:** *In present trend of integration will continue in the projected future. When comparing the integration density of integrated circuits, a clear distinction must be made between the memory chips and logic chips. Memory circuits are highly regular. Increase of chip complexity is consistently higher for memory circuits. The salient features such as low power, reliable performance, circuit techniques for high speed such as using dynamic circuits, and low leakage current, most of these have get give a better advantage. This paper gives an idea about 4T DRAM (dynamic random access memory) which is implemented by using a self controllable voltage level technique. In this technique reduces the leakage current and produce the high performance. Simulation is done by using a microwind 3.1 and DSCH3. Using a 90 nm technology to implemented a 4T DRAM. By using this give the benefit of 67% reduction of leakage current. This reduction gives a advantage of high performance and low leakage current, by controlling these parameter speed is automatically increase.*

**Keywords:** *low leakage current, self controllable voltage level technique, low power. high performance, high speed.*

### **I. Introduction**

Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital systems. The amount of memory required in a particular system depends on the type of application, but, in general, the number of transistors utilized for the information (data) storage function is much larger than the number of transistors used in logic operations and for other purposes. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development towards more compact design rules and, consequently, toward higher data storage densities. Thus, the maximum realizable data storage capacity of single-chip semiconductor memory arrays approximately doubles every two years. On-chip memory arrays have become widely used subsystems in many VLSI circuits, and commercially available single-chip read/write memory capacity has reached 64 megabits. This trend toward higher memory density and larger storage capacity will continue to push the leading edge of digital system design.

The area efficiency of the memory array, i.e., the number of stored data bits per unit area, is one of the key design criteria that determine the overall storage capacity and, hence, the memory cost per bit. Another important issue is the memory access time, i.e., the time required to store and/or retrieve a particular data bit in the memory array. The access time determines the memory speed, which is an important performance criterion of the memory array. Finally, the static and dynamic power consumption of the memory array is a significant factor to be considered in the design, because of the increasing importance of low-power applications. In the following, we will investigate different types of MOS memory arrays and discuss in detail the issues of area, speed, and power consumption for each circuit type Read-write (R/W) memory circuits, on the other hand, must permit the modification (writing) of data bits stored in the memory array, as well as their retrieval (reading) on demand. This requires that the data storage function be volatile, i.e., the stored data are lost when the power supply voltage is turned off. The read-write memory circuit is commonly called Dynamic Random Access Memory (RAM), mostly due to historical reasons. Compared to sequential-access memories such as magnetic tapes, any cell in the R/W memory array can be accessed with nearly equal access time.

I have design a 4T DRAM and implement by using a self controllable voltage level technique and simulate in microwind 3.1. To access a particular memory cell, i.e., a particular data bit in this array, the corresponding bit line and the corresponding word line must be activated (selected). The row and column selection operations are accomplished by row and column decoders, respectively. The row decoder circuit selects one out of  $2^N$  word lines according to an  $N$  bit row address, while the column decoder circuit selects one out of  $2^M$  bit lines according to an  $M$ -bit column address. Once a memory cell or a group of memory cells are selected in this fashion, a data read and a data write operation may be performed on the selected single bit or multiple bits on a particular row. The column decoder circuit serves the double duties of selecting the particular columns and routing the corresponding data content in a selected row to the output.

## II. History of work

Number of paper investigating and get conclusion. The time-shared processing elements for VLSI implementations that minimizes the overall power dissipation is shown in [1]. Miniaturized MOSFET's with channel lengths even shorter than one tenth of a micrometer could probably be realized with superior performance [2]. The power reducing parameter shown in [3]. The leakage reduction method based on the selective insertion of control points has developed [4]. Techniques that reduce total leakage in circuits operating in the active mode at different temperature conditions are examined in [5]. The sleepy stack incurs some delay and area overhead the sleepy stack technique achieves the lowest leakage power consumption among known state-saving leakage reduction techniques shown in [6]. New technique for reducing the leakage current of CMOS circuits is proposed and makes use of the fact that leakage currents of gates are depended on their input patterns in [7]. Paper evaluates and compares the different static logic styles with dual threshold voltage and power gating techniques to attain low power and high performance VLSI systems in terms of power delay product and standby leakage power in [8]. The paper propose a novel circuit technique using depletion mode devices, to reduce the static energy of SRAM array in an on-chip cache by 90% without any performance impact in [9]. The paper proposes a new high-performance bipolar CMOS-merged technology DRAM [10].

## III. Proposed work

As the trend for high-density DRAM arrays forces the memory cell size to shrink, alternative data storage concepts must be considered to accommodate these demands. In a dynamic RAM cell, binary data is stored simply as charge in a capacitor, where the presence or absence of stored charge determines the value of the stored bit. The data stored as charge in a capacitor cannot be retained indefinitely, because the leakage currents eventually remove or modify the stored charge. Thus, all dynamic memory cells require a periodic refreshing of the stored data, so that unwanted modifications due to leakage are prevented before they occur. The use of a capacitor as the primary storage device generally enables the DRAM cell to be realized on a much smaller silicon area compared to the typical SRAM cell. Notice that even as the binary data is stored as charge in a capacitor, the DRAM cell must have access devices, or switches, which can be activated externally for "read" and "write" operations. But this requirement does not significantly affect the area advantage over the SRAM cell, since the cell access circuitry is usually very simple. Also, no static power is dissipated for storing charge on the capacitance. Consequently, dynamic RAM arrays can achieve higher integration densities than SRAM arrays. Note that a DRAM array also requires additional peripheral circuitry for scheduling and performing the periodic data refresh operations. The hardware overhead of the refresh circuitry, however, does not overshadow the area advantages gained by the small cell size.

### A. 4T Dynamic memory cell

Figure 1 shows schematic of 4T DRAM in which the read and write operation is performed when M3 and M4 ON. If M3 and M4 off, read and write operation is not performed.

The steady-state voltage:  $V_{Cc} = V_{DD} - V_T$

(i) Write "1" operation ( $W_L = 1$  - M3, M4 on)  $V_C$  - forced to 0 by data write circuitry,  $V_2$  decreases to 0, M1 off;  $V_1$  increases; Final state:  $V_1 = 1$ ,  $V_2 = 0$

(ii) Read "1" operation ( $W_L = 1$  - M3, M4 on) M1 off; M2, M4 on;  $V_C$  - pulled down,  $V_C > V_C$  read as a logic "1"

(iii) Write "0" operation ( $W_L = 1$  - M3, M4 on)  $V_C$  - forced to 0 by data write circuitry,  $V_1$  goes to 0, M2 off;  $V_2$  increases to 1 Final state:  $V_1 = 0$ ,  $V_2 = 1$

(iv) Read "0" operation ( $W_L = 1$  - M3, M4 on) M2 off; M1, M3 on;  $V_C$  - pulled down,  $V_C < V_C$  read as logic 0

The layout of 4T DRAM is shown in figure 2 in this diagram shows a NMOS is implemented by using a n+ diffusion layer and gate is implemented by using a polysilicon and interconnects are implemented by using metal1 and metal 2.

Waveform of 4T DRAM is shown in figure 3. The read and write operation is shown. The read and write operation is activated when the word line is active in condition. If word line is not active condition circuit behaves as an open circuit .the leakage current in this time occur a 0.566ma and this is shown in diagram 4. the leakage current is the major factor to disturb the circuit behavior.

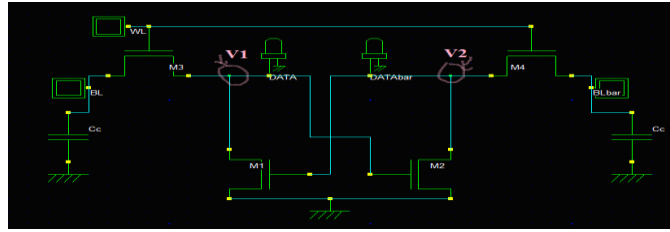


Figure 1 shows schematic of 4T DRAM

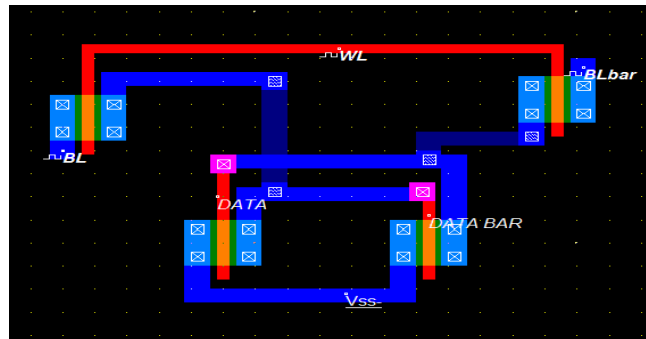


Figure 2 shows a layout of 4T DRAM

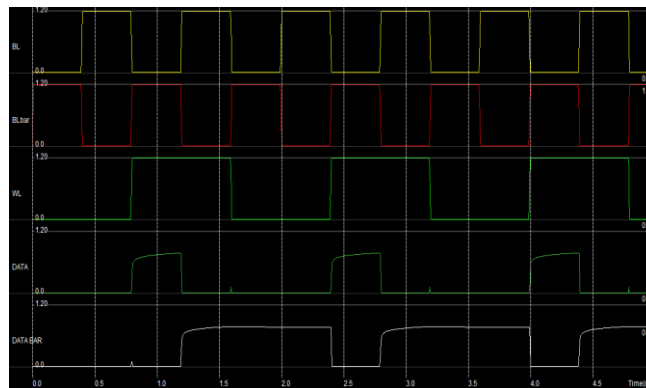


Figure 3 shows a waveform of 4T DRAM voltage versus time

To remove the leakage current in the circuit have used a self controllable voltage level (SVL) technique. The 4T DRAM is implemented by using a SVL technique. The SVL technique is divided by using a upper SVL and lower SVL. The upper SVL connected to the upper side of the circuit and lower SVL connected to lower side of the circuit. This is shown in the figure 5. The self controllable voltage level provides a maximum DC voltage to an active load. The upper SVL consist of one NMOS and one PMOS. The parallel combination of the NMOS and PMOS connected to series of the circuit and one side connect the VDD and other side connected to circuit. Similarly the lower SVL is combination of NMOS and PMOS in which the one side is connected to the ground-level power supply (VSS) and other side is connected to the circuit.

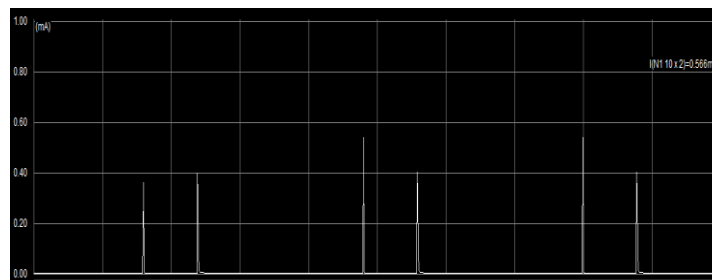


Figure 4 shows the leakage current waveform of 3T DRAM

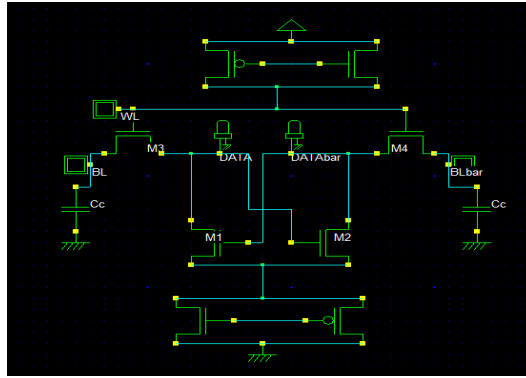


Figure 5 shows schematic of 4T DRAM with self controllable voltage level

Now layout diagram 4T DRAM with SVL technique is shown in figure 6. The read and write operation waveform is shown in 7. To implement the circuit with SVL technique reduce the leakage current of 67%. To simulate these use a 90nm technology. MOS circuit is formed on four basic layers – n-diffusion, p-diffusion, poly silicon, and metal, which are isolated from one another by thick or thin silicon dioxide insulating layers. In some processes there may be a second layer and also in some processes a second poly silicon layer. Layers may deliberately join together where the contact form.

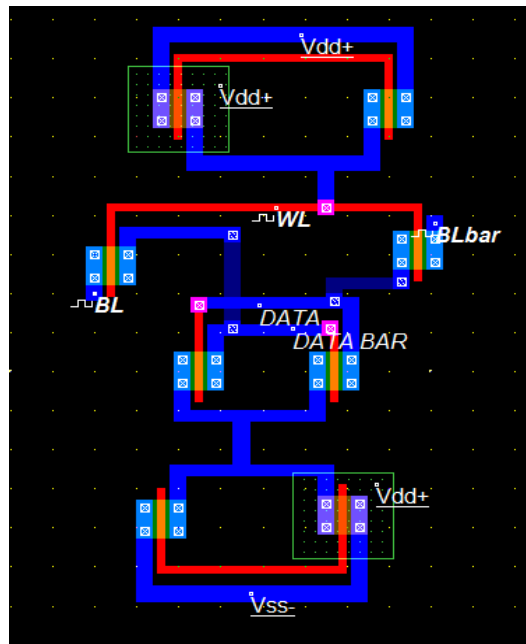


Figure 6 shows a layout of 4T DRAM with self controllable voltage level

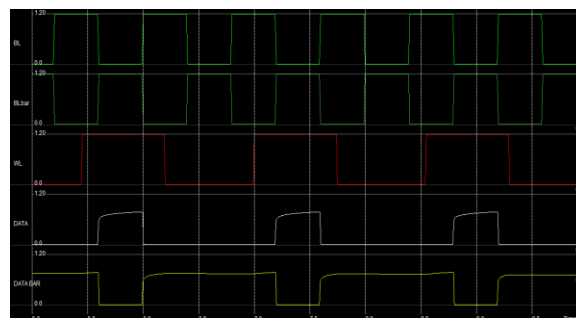


Figure 7 shows a waveform of 4T DRAM with self controllable voltage level

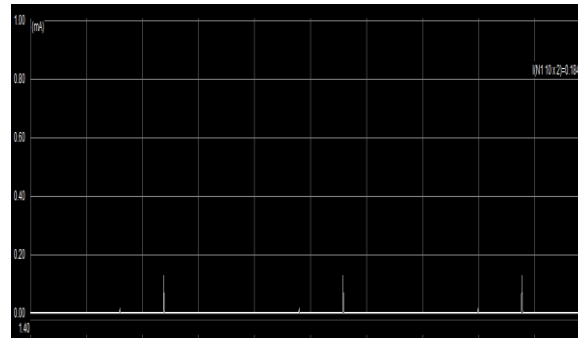


Figure 8 shows the leakage current waveform of 4T DRAM with self-controllable voltage level

#### IV. Circuit simulation result

The simulation of 4T DRAM with self-controllable voltage level is done by using a microwind 3.1 and DSCH 2, in which used a number of layers. The 90nm technology is considered in which 6 metal copper strained SiGe is used at temperature 27°C. The table –I shows a 90nm technology parameters of 4T DRAM. The table –II shows a simulation result of 4T DRAM. total dynamic power dissipation in the circuit is 0.191mw.

Table –I Parameter of 4T DRAM

| Process technology   | 90nm |
|----------------------|------|
| Power supply voltage | 1.2v |
| Pre charge voltage   | 1v   |

Table –II Simulation result of SVL based 4T DRAM

| Circuit                        | Leakage current |
|--------------------------------|-----------------|
| 4T dram during write operation | 0.566ma         |
| 4T DRAM with SVL               | 0.184ma         |

#### V. Conclusions

4T DRAM with self-controllable voltage level is implemented by using a microwind 3.1 and DSCH 2. it's a beneficial for reduction up to 67% of the leakage current. To reduce these improve the performance and speed of the design. The power supply (VDD) is used 1.2v. Here 90nm technology is used. To implement these technology power dissipation is also reduced. Its also improved further by change in width to length ratio.

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