



SRAM CELL MODELING FOR READ STABILITY AND WRITE ABILITY

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Abstract- Read stability/static noise margin (SNM) and write ability are two important parameters of a memory cell. These parameters are analyzed for various technologies i.e. tsmc350, tsmc250, tsmc180. Memory cell behaviour with different cell ratio and pull ratio has been analyzed, which are design parameters. Write margin (WM), determines how easily a memory cell can be written NCURVE METHOD is used to determine the stability of the cell in terms of current. Scaling of supply voltage has great effect on power dissipation, speed as well as reliability of SRAM Cell. N-CURVE METHOD and SWEEP METHOD have been used for measuring read and write stability of SRAM cell.

Keywords- SNM, WNM, SVN, SINM, WTV & WTI

I. Introduction

CMOS (complementary metal oxide semiconductor) technology has been extensively used in digital integrated circuits because of their intrinsic features in low-power consumption, large noise margins, and ease of design. Therefore CMOS integrated circuits have been widely used to develop random access memories (RAMs). SRAM 6-T cell represents cross coupled inverters having infinite gain, with access transistors having bit lines and word lines [1]. Single port 6T SRAM is used as cache memory on the processor chip because of its high speed. Mainly this work is presented for 180nm technology. The stability of SRAM cell can be characterized by static noise margin, write margin and read current (performance)[1]. These parameters are mainly defined by design constraints cell ratio and pull up ratio [1][8]. Cell ratio is defined as the ratio of driver and access transistor, However pull up ratio is the ratio of pull up device and access transistor [9].

In this paper, the effect of process parameters like Temperature, V_{dd} and Technology variations has been characterized for the reliability of SRAM cell. Stability of SRAM cell becomes susceptible at low supply voltage [6]. Since as the device dimension goes to nanoscale, the intrinsic parameter fluctuation results in variation in V_{th} which makes the SRAM cell design less predictable and controllable [7]. Hence even two transistors integrated on same chip don't have same electrical characteristics.

II. Read stability of SRAM Cell

Static noise margin (SNM) / Read margin is the dc noise that can be tolerated by SRAM cell. It is the maximum noise that can be tolerated at storage nodes without flipping the content of cell [1][9]. Here, cross coupled inverters are presented with static noise sources V_n [1](static noise is the dc disturbance such as offsets and mismatches due to process variation and operating conditions) as in figure1(a). During read operation the bitlines are precharged to V_{dd} shown in Figure1 (b). Storage nodes of cell represent two states 0 and 1, configured with access transistors and bitlines. So, discharging of bit line voltage associated with storage node '0' is sensed by sense amplifier and read operation can be performed. The SNM can be determined by finding maximum possible square from butterfly curves (VTC curve) [3]. SNM/Read margin is mainly characterized by cell ratio, larger it is larger the value of SNM. But area is also an important parameter while designing, SNM is limited by V_{dd} and write margin [1][3].

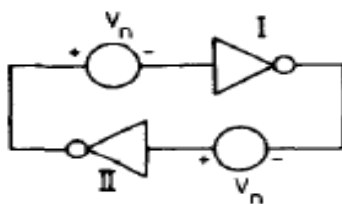


Figure 1(a): Cross coupled inverters having noise sources.

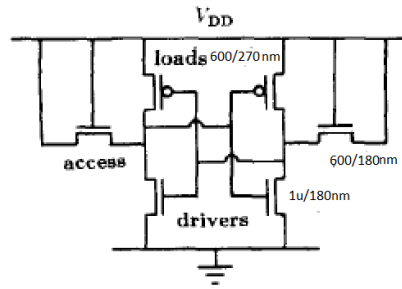


Figure 1(b): Read configuration of SRAM cell

III. Write ability of SRAM cell

Write noise margin, WNM is defined as the minimum bit line voltage required for flipping the state of SRAM cell [4]. Write margin has been calculated using SWEEP METHOD [10], both the bitlines are applied with V_{dd} and ground at storage nodes '0' and '1' correspondingly. Voltage sweep from V_{dd} is made and write margin can be calculated as in Figure 2. Write margin is mainly characterized by pull up ratio of the cell, larger the pull up ratio smaller the write margin will be and cell ratio must be smaller. Hence both SNM and WNM have opposite behaviour [1], so if the cell is designed for better SNM, the WNM would be degraded. SNM and WNM are function of threshold voltages of driver transistors.

IV. SVN, SINM, WTV & WTI

Above discussion shows read stability and write ability in terms voltages only. But using N-Curve Method [1] we can characterize the stability of SRAM cell in terms of current. Two cells of same SNM and SVN doesn't mean that they are equally stable, the cell which have larger

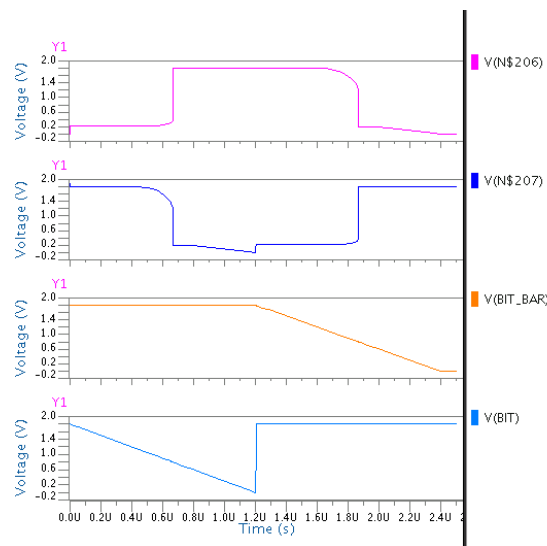


Figure 2: VTC curve with bit line voltages during write operation at 1.8V

Value of current is more stable. For extracting N-curve both the bitlines are clamped to V_{dd} for read operation of SRAM cell shown in Figure 3. External voltage source " V_{in} " applied at storage node 0, is made sweep from 0 to V_{dd} and corresponding current I_{in} has been measured.

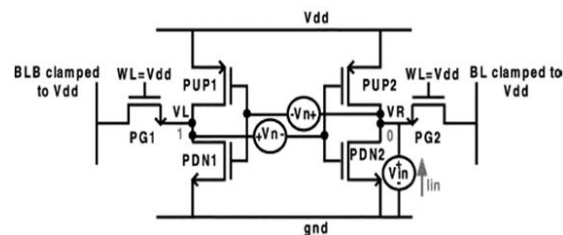


Figure 3: Configuration of SRAM cell using N-curve method

SVNM/static voltage noise margin is the maximum DC noise voltage at storage node of the bit cell before its content changes. Points A and C are two stable points of butterfly curve, B is metastable point as in Figure 4. The voltage difference between A and B shows maximum tolerable DC noise voltage before flipping of content of cell, it is SVNM and peak of current is SINM (Maximum current injected in SRAM cell before the flipping of content of cell) which is -ve due to its direction. The voltage difference between B and C shows write trip voltage/WTV. For a write operation bitlines voltage has been pulled from V_{dd} to ground that discharges '1'.

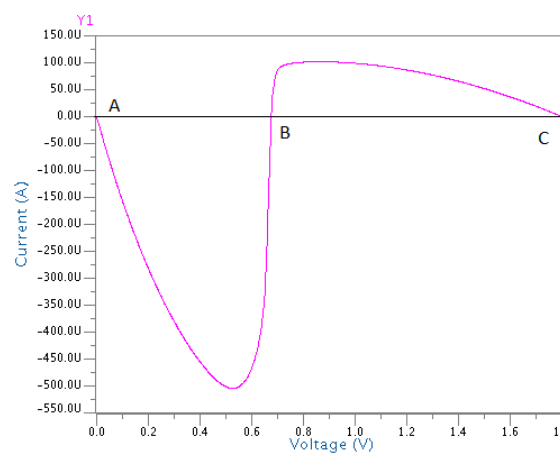


Figure 4: Current through voltage source shows read and write margin using N-Curve

WTI is the amount of current needed to write the cell when both bitlines are clamped at V_{dd} . The cell have small value of SVNM with larger SINM is also stable because value of charge that is to be discharged is large during write operation.

V. Parameters that effects Read stability and Write ability

A. Cell Ratio

Read margin is mainly characterized by cell ratio. Large the value of cell ratio high will be the SNM [9] because of less bump voltage at storage node '0'. Strong driver transistor and weak access transistor is preferable for better SNM.

The graphical representation of different parameters with cell ratio is provided in Figure 5(a), 5(b) & 5(c).

B. Pull up Ratio

Write margin can be directly characterized by pull up ratio [1]. As pull up ratio increases, WNM gets reduced, so pull up ratio should not be increases beyond certain limit. For better WNM pull up device (PMOS) should weak but access transistor (NMOS) should be strong.

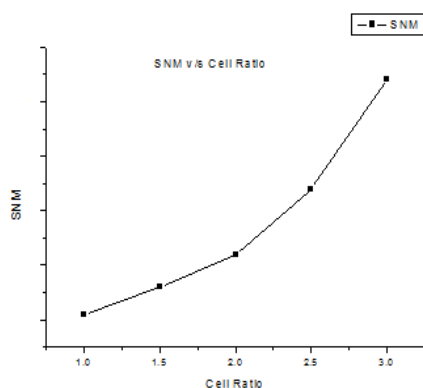


Figure 5(a): SNM v/s Cell Ratio

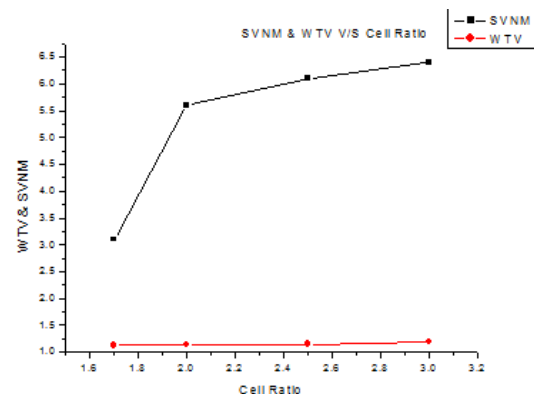


Figure 5(b): SVNM v/s cell ratio

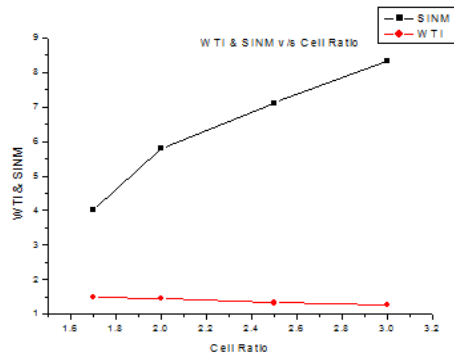


Figure 5(c): WTI & SINM v/s Cell Ratio

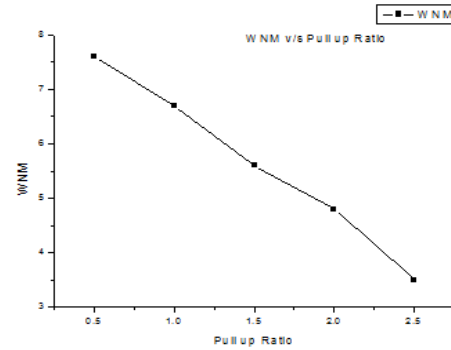


Figure 6(a): WNM v/s pull up ratio

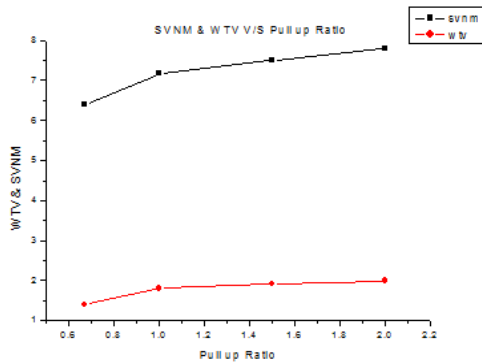


Figure 6(b): WTV v/s Pull up ratio

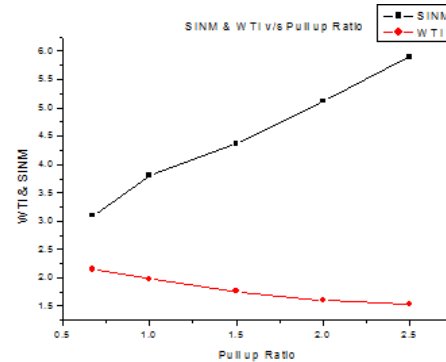


Figure 6(c): WTI & SINM v/s Pull up Ratio

The graphical representation of different parameters with pull up ratio is provided in Figure 6(a), 6(b) & 6(c).

C. Supply Voltage

Read operation becomes destructive write at very low voltages. Hence, at very low V_{dd} (approaching to V_{th}) the characteristic degrades represented in 7(a). Scaling of supply voltages is made to reduce power dissipation shown in 7(b), but this increases leakage [3][4]. Also scaling of V_{dd} reduces the speed [6] to a great extent. Read and Write margins are limited to $0.5V_{dd}$ [1]. SNM, WNM, SVNM, SINM & write time variation with scaled V_{dd} have been represented in 7(c), (d), (e), (f) & (g).

As the device dimensions goes to nanoscale in today's VLSI environment i.e as technology varies from 350nm to 180nm (Same V_{dd}) speed of cell gets improved but power dissipation gets increased. So for low power applications, we need to scale supply voltage to reduce power consumption [5].

D. Temperature

This paper presented the simulation of cell at various temperatures (-40° , 27° , 125°). SNM reduces as temperature increases [3] as in Figure 8(a). WNM increases when temperature increases from -40° to 125° as in Figure 8(b). SRAM cell's speed gets increased with temperature i.e. write time decreases with increase of temperature.

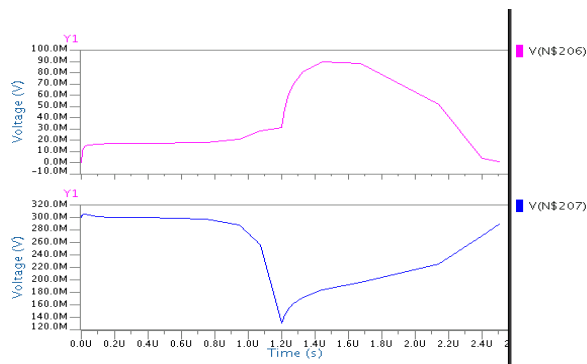
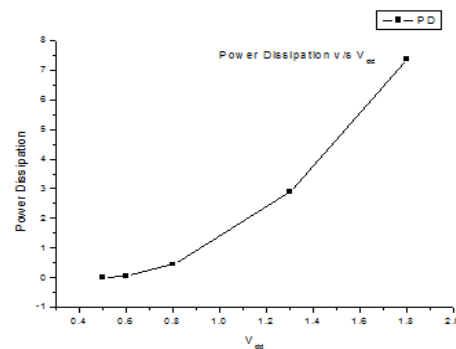


Figure 7(a): Degraded VTC curve at 0.4V

Figure 7(b): Power Dissipation v/s V_{dd}

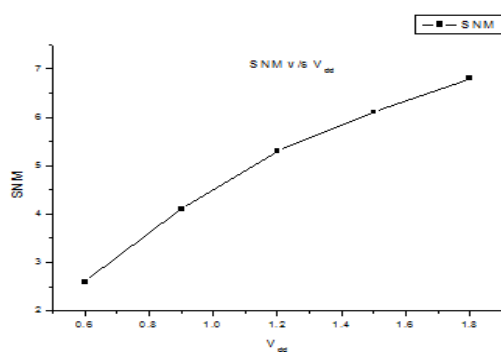


Figure 7(c): SNM with V_{dd}

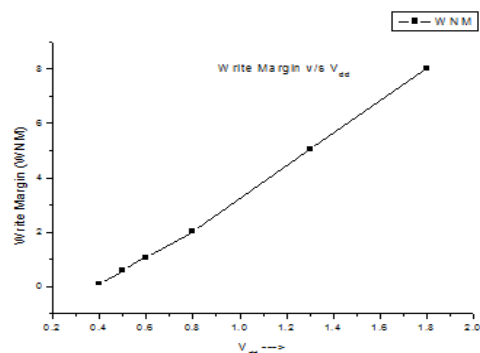


Figure 7(d): WNM v/s V_{dd}

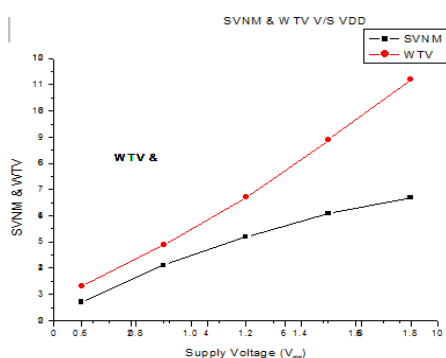


Figure 7(e): SVN, SINM v/s V_{dd}

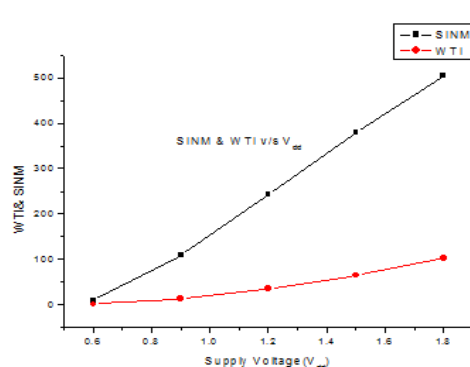


Figure 7(f): WTV, WTI v/s V_{dd}

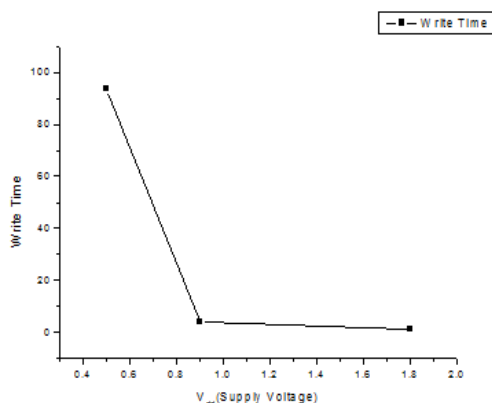


Figure 7(g): Write time v/s V_{dd}

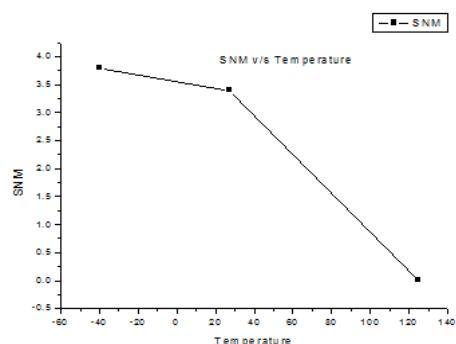


Figure 8(a): SNM v/s Temperature

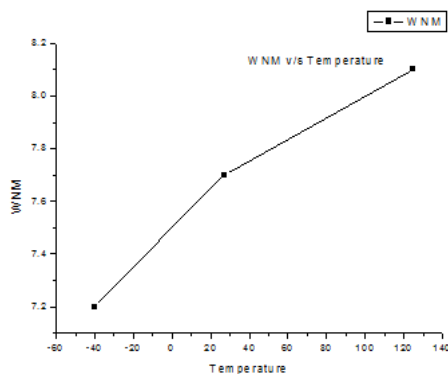


Figure 8(b): WNM v/s Temperature

E. Technology Variation

As the technology is growing, the device dimension is reducing, leads to fluctuation of intrinsic process parameters (random dopant density variation in channel, drain & source) which results in variation of V_{th} [7]. Hence this variation affects SRAM cell stability to great extent. SNM reduces as we move from 350nm to 180nm technology. The stability of SRAM cell being the critical issue when technology reaches 20-22nm. Write time also reduces with technology.

VI. Conclusion

This paper reveals the stability of SRAM cell with various intrinsic & extrinsic process parameters (V_{dd} & Temperature) [3]. As the trend moves to nanoscale devices the stability becomes critical issue due to leakage current and V_{th} variations. If two cells having same cell ratio and pull up ratio but one shows higher stability, which is having current driving capability larger than other [1]. Hence SVN, SIN, WTV & WTI represent correct results for stability of SRAM cell.

VII. Future Work

Scaling of the device dimensions has great impact on the stability of the bit cell or memory. We can include these variation impact in simulation by using "Monte-Carlo Simulation", which is based on the random-variables.

Future work also involves the multiple threshold voltage (v_{th}) design in which we can use the devices with different v_{th} in the same design. The advantage of this approach is that in critical path where speed is main concern, we can use low v_{th} device. But in non critical path, we can use high v_{th} devices so that we can save power. So this type of approach will increase the speed without affecting the power consumption much more. One method to control the threshold voltage is by using body biasing. "Thus, maintain the stability of the SRAM cell on the upcoming technologies like (22, 20nm) is the further topic of research". Ideas from theory revision might turn out to be useful in this context.

References

- [1]. Evelyn Grossar, Michele Stucchi, Karen Maex, and Wim Dehaene, "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometre Technologies", IEEE Journal of Solid State Circuits, November 2006.
- [2]. Ken'ichi Agawa, Hiroyuki Hara, Toshinari akayanagi, and Tadahiro Kuroda "A Bitline Leakage Compensation Scheme for Low-Voltage SRAMs", IEEE journal 2001.
- [3]. Benton H. Calhoun and Anantha Chandrakasan, "Analyzing Static Noise Margin for Sub-threshold SRAM in 65nm CMOS" Proceedings of ESSCIRC, 2005
- [4]. Koichi Takeda, Yasuhiko Nomura, "A Read-Static-Noise-Margin-Free SRAM Cell for Low- V_{dd} and High-Speed Applications", IEEE January 2006
- [5]. James S. Caravella, "A Low Voltage SRAM for Embedded Applications", IEEE Journal 1997
- [6]. Ricardo Gonzalez, Benjamin M. Gordon, and Mark A. Horowitz, "Supply and Threshold Voltage Scaling for Low Power CMOS", IEEE 1997
- [7]. Azeez J. Bhavnagarwala & Xinghai Tang, "The Impact of Intrinsic Device fluctuations on CMOS SRAM Cell Stability", IEEE journal 2001.
- [8]. Evert Seevinck, F. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cell", IEEE J. Solid-State Circuits, October 1987
- [9]. B. Alorda, G. Torrens, S. Bota and J. Segura, "Static-Noise Margin Analysis during Read Operation of 6T SRAM Cells" Univ. de les Illes Balears, Dept. Fisica, Cra. Valldemossa, km. 7.5, 07071 Palma de Mallorca, Spain.
- [10]. Jiajing Wang, Satyanand Nalam, and Benton H. Calhoun, "Analyzing Static and Dynamic Write Margin for Nanometer SRAMs", Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA 22904, USA