



A Novel Power and Area Efficient 4-bit Flash ADC Using Multiplexers

Mrs. Jasbir Kaur¹, Mr. Saurabh Kansal²

Assistant Professor, ECE Department, PEC University of Technology, Chandigarh, India¹

PG Scholar, Electronics (VLSI Design), PEC University of Technology, Chandigarh, India²

Abstract: This paper presents a 4 bit flash ADC that has been designed using CMOS technology of GPDK 180nm. The architecture used in this ADC is advanced from the conventional flash ADC. The proposed flash ADC uses less comparator as compared to conventional flash ADC. Simulation on Cadence analog tool (Virtuoso) results show that power and area (in the terms of transistor count) of designed flash ADC has been reduced significantly as compared to conventional flash ADC. Power has been reduced by 43% and number of transistors has been reduced by 59.8% using this architecture.

Keywords: Flash ADC, Multiplexers, comparator, sample and hold circuit, Cadence tool

I. Introduction

In this modern era of digitization, almost all the applications needs digital output because it is easy to store and understand it. Flash ADC suits most of the application that requires medium to high conversion time and resolution but the problem with flash ADC is that it requires large area. In this paper, presented flash ADC is designed using multiplexers that reduce the area in the terms of transistors count and also reduce the power consumed. This 4 bit flash ADC uses six comparators instead of fifteen comparators therefore area and power get reduced. The paper is organized as follows. A brief introduction about flash ADCs is given in Section I. In section II, the conventional ADC architecture has been discussed. In section III, the designed flash ADC with its components has been explained briefly. In section IV, Simulation results and comparison of conventional flash ADC versus designed ADC is done. Finally, conclusion is given in section V.

II. Conventional Flash ADC

A conventional flash ADC consists of potential divider network, comparators, and encoder as shown in Fig 1. The reference voltage is divided into equally spaced values by potential divider network which consists of 16 resistors of equal value. Thus, with the help of resistors network, we obtain 15 different reference voltage levels, each of which is fed to comparator. The analog input which is to be converted is compared with these 15 different reference values to generate a thermometer code [3].

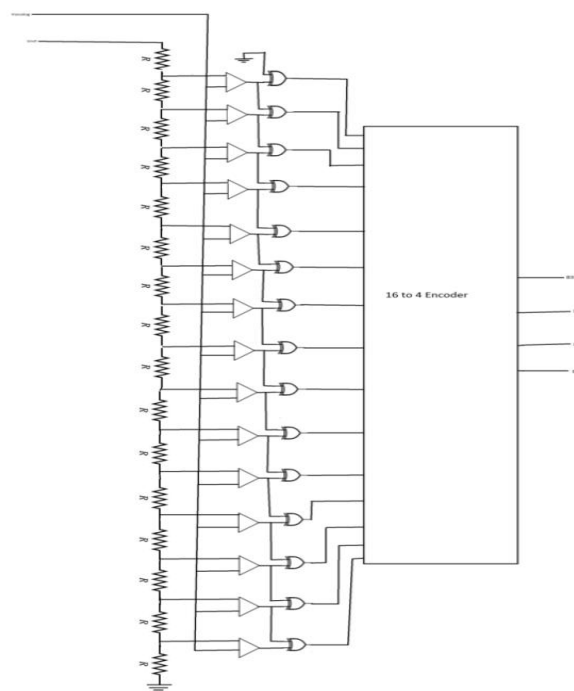


Fig. 1. Block Diagram of Conventional 4 bit Flash ADC

Flash ADC consists of a series of comparators, each one comparing the input signal to a unique reference voltage. Generally, the comparator outputs are given to the inputs of priority encoder, which convert the thermometric codes into binary output. But in the above ADC comparator outputs are given to the inputs of EX-OR gate ladder which produces a code which can easily be converted into binary output using 16 to 4 bit encoder [10]. Traditional flash ADC architecture uses 2^N resistors and $2^N - 1$ comparator. These $2^N - 1$ comparators will work in parallel, which will cause high power consumption. The component count of a flash ADC grows exponentially with resolution. Therefore, the area and power consumed by the ADC circuit increase exponentially with resolution.

III. Designed ADC Architecture

The major disadvantage of the conventional flash ADC is its high chip area, high power consumption and high input capacitance. The four bit flash ADC using multiplexer has much lesser area and less power consumption. The architecture of the designed ADC is shown in fig. 2.

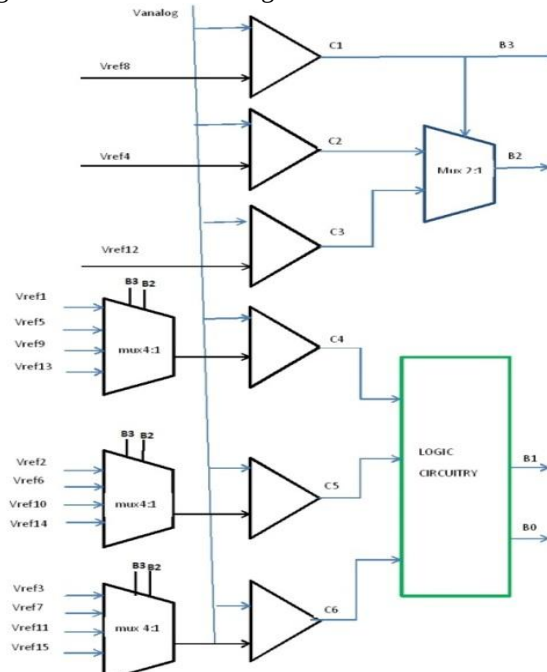


Fig. 2. Block Diagram of four bit Flash ADC using Multiplexer

Main components of this ADC include Sample and Hold circuit, Comparator, Multiplexer 4:1, Multiplexer 2:1 and logic circuitry. Analog input given to the ADC through sample and hold circuit not shown in the block diagram. This input goes to the non-inverting input of comparator C1, C2 and C3 and inverting inputs are connected to $8V_{ref}/16$, $4V_{ref}/16$, and $12V_{ref}/16$ respectively to generate the MSBs. The outputs of comparators are used to control the output of Multiplexer 2:1. Thus, B3 and B2 are decided by the outputs of comparators C1, C2, C3 and Multiplexer 2:1.

Table I: Outputs B3 and B2 corresponding to VIN

C1 acts the select line and Output bit B3. C2 and C3 are the inputs of Mux. B2 is the output of Mux.					
Vin	C1	C2	C3	B3	B2
$0 < V_a < V_{ref4}$	0	0	0	0	0
$V_{ref4} < V_a < V_{ref8}$	0	1	0	0	1
$V_{ref8} < V_a < V_{ref12}$	1	1	0	1	0
$V_{ref12} < V_a < V_{ref16}$	1	1	1	1	1

The outputs B3 and B2 are connected to select line of each of the Multiplexer 4:1, this leads to appropriate Vref at the input of comparator C4, C5 and C6. The outputs of the comparator C4, C5 and C6 decide the output binary bits B1 and B0. Thus, the design of the flash ADC uses 6 comparators and some extra overhead of multiplexers instead of 15 comparator, 16 EXOR gates and encoder of conventional flash ADC. Thus, it reduces area and power consumed. Generally, this type of architecture uses $2^{(N-2)} + 2$ comparators instead of $2^N - 1$ comparators which are very less in number [1].

A. Comparator

Comparator used in ADCs plays very critical role. The parameters such as input offset voltage, propagation delay, power consumption and input range of comparator decides the critical parameters of flash ADC.

Comparator consumes considerable power in ADC circuits. As the resolution increases, the number of comparator increases and consequently, the power consumed and area also increases exponentially. At high frequencies, the noise generated in the comparator is considerable. Block diagram of comparator used in designed ADC is shown in fig.3.

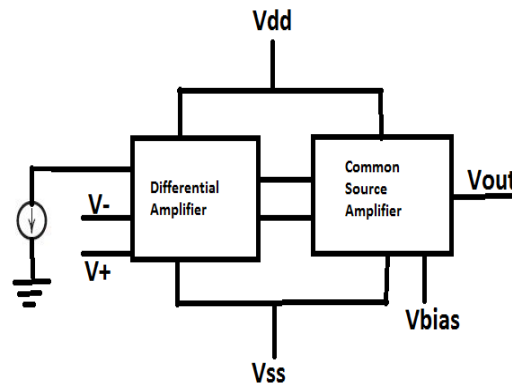


Fig. 3. Block diagram of Comparator

Comparator used in flash ADC is designed using CMOS technology so that it consumes minimum power. It consists of two stages (i) Differential amplifier (ii) Common source amplifier

(i). *Differential Amplifier*

The active loaded MOS differential amplifier schematic is shown in fig 4. It consists of two matched transistors, NM0 and NM1, whose sources are joined together and biased by a constant-current source I . The constant current source is usually implemented by a MOSFET circuit of current mirror. Generally, each drain of differential amplifier is connected to the positive supply through a drain resistance, but active (current-source) loads are employed here. Whatever type of load is used, it is essential that the MOSFETs not enter the triode region of operation.

Transistor NM0 and NM1 are biased using constant current source which has been implemented using a current mirror circuit i.e. source of NM0 and NM1 are connected to each other and current source is applied to them. Current mirror has been implemented using NM2 and NM3. PM0 and PM1 are used as an active load also acts as a current mirror.

$$\text{Differential gain} = \frac{V_{out}}{V_1 - V_2} \quad \text{and} \quad A_d = \frac{1}{2} g_m r_0$$

Where A_d represents the differential gain of the differential amplifier, g_m denotes the transconductance of MOS transistor and r_0 denotes the output resistance of MOS transistor.

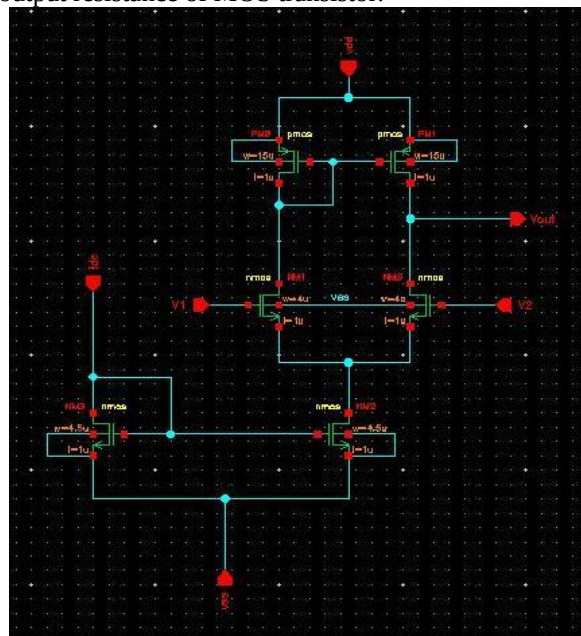


Fig.4. Circuit Diagram of Differential amplifier

Current Mirror

The circuit of a simple MOS constant-current source is given by fig 5.

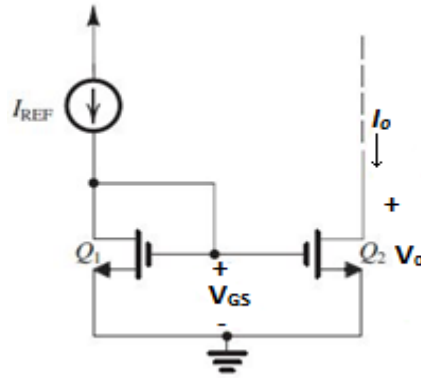


Fig.5. Current mirror circuit

The heart of the circuit is transistor Q1, the drain of which is shorted to its gate, thereby forcing it to operate in the saturation mode with

$$I_{D1} = \frac{1}{2} k_n' \frac{(W)_1}{(L)_1} (V_{GS} - V_{tn})^2$$

The drain current of Q1 is supplied by current source, which in most cases would be outside the IC chip. Since the gate currents are zero where the current of current source is considered to be the reference current of the current source and is denoted I_{REF} .

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

Now consider transistor Q2: It has the same as Q1; thus, if we assume that it is operating in saturation, its drain current which is the output current of the current source I_O , will be

$$I_O = I_{D2} = \frac{1}{2} k_n' \frac{(W)_2}{(L)_2} (V_{GS} - V_{tn})^2$$

The special connection of Q1 and Q2 provides an output current I_O that is related to the reference current I_{REF} by the aspect ratios of the transistors. In other words, the relationship between I_O and I_{REF} is solely determined by the geometries of the transistors.

$$\frac{I_O}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1}$$

(ii). Common Source Amplifier

The Schematic of the Common Source Amplifier is shown in the fig. 6

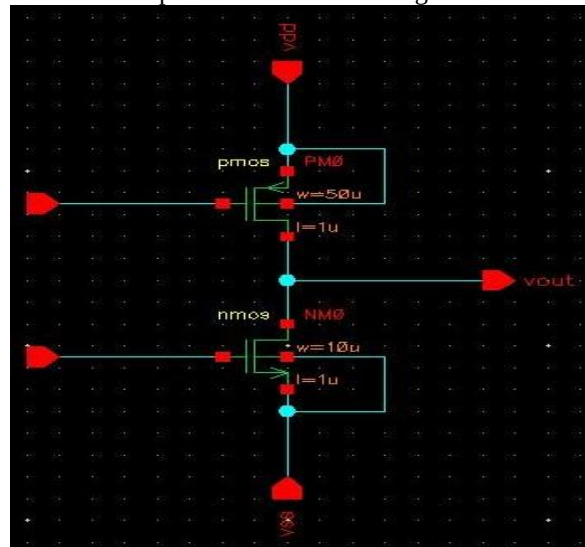


Fig. 6. Schematic of Common Source Amplifier

As shown in the schematic, the input to CS amplifier is given between source and gate terminal of NMOS and output is taken between source and drain of NMOS. PMOS acts as active load and input given to it keeps the amplifier in saturation region. The input of CS amplifier is the output of differential amplifier and gain of the CS

amplifier is such that if the difference between V_1 and V_2 applied to the differential amplifier is positive then output saturates to the $+V_{DD}$ otherwise $-V_{DD}$.

B. MUX 2:1

CMOS transmission gates provide an efficient way to build steering logic. Steering logic circuits are circuits that route data inputs to outputs based on the settings of control signals. Transmission gates implementation is shown in fig. 7 and fig. 8.

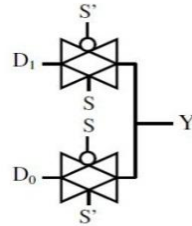


Fig.7. Mux 2:1 using Transmission gate

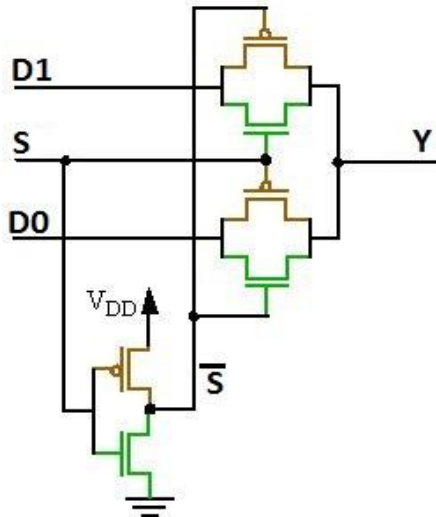


Fig. 8. Schematic of Mux 2:1

Number of transistor required for Mux 2:1 using logic Gates = 20

Number of transistor required for Mux 2:1 using transmission gates = 6

The main advantage of using transmission gate in Mux implementation is that the number of the transistor used has reduced significantly.

C. MUX 4:1

Mux 4:1 has been implemented using transmission gates. It has been implemented using mux 2:1 as show in the fig. 9 and fig 10.

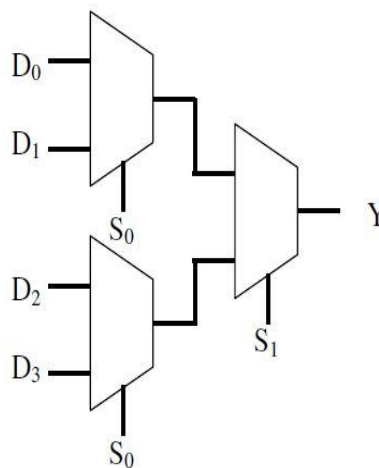


Fig.9. Symbol Schematic of Mux 4:1

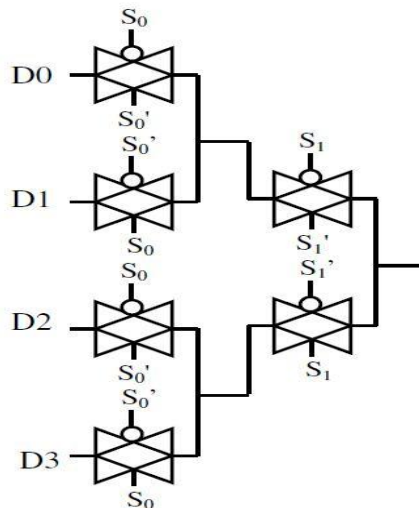


Fig.10. Mux 4:1 using Transmission gate

Number of transistor required for Mux 2:1 using logic Gates = 34

Number of transistor required for Mux 2:1 using transmission gates = 22

IV. Simulation and Experimental Results

Simulation of the conventional four bit Flash ADC and designed Flash ADC using multiplexers have been done with Cadence Analog tool using 180 nm technology at schematic level. For the simulation purpose, an input analog signal of 1.2 V, 1 KHz with a DC level of 1.2 V has been used. Transient analysis has been done for a period of 1ms. The sampling period used is 64 μ s. In the outputs results Vanalog, Vhold and B1, B2, B3, B4 has been plotted. Simulation results have been shown in fig.11 and fig.12. The average power consumed and number of transistors used has been compared is shown in comparison table II.

Table II: Comparison of power consumed and area

Spec.	Arch.	Conventional Flash ADC	Multiple selection flash ADC(Designed)
Technology		GPDK 180nm	GPDK 180nm
Power Supply		3.3V	3.3V
Resolution		4 bit	4 bit
Input Analog Range		0~2.4V	0~2.4V
Power Consumed		11.23mW	6.40mW
Area (in terms of transistor count)		304	122

V. Conclusion

The proposed flash ADC consumes less power and less area. The flash ADC designed with multiplexer consume 6.40mW power while conventional flash ADC consume 11.23mW and the number of transistor used in flash ADC designed with multiplexer is 122 while conventional flash ADC uses 304 transistor. Thus, this designed ADC is both power and area efficient.

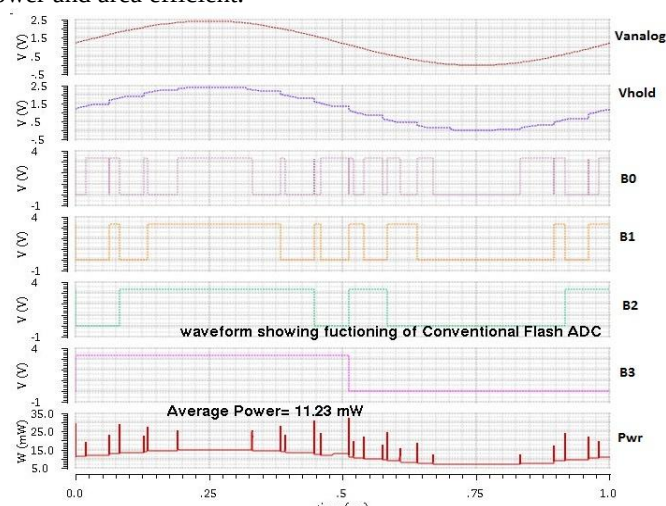


Fig. 11. The Simulation results of Conventional Flash ADC (Vsin= 1.2V at DC 1.2V)

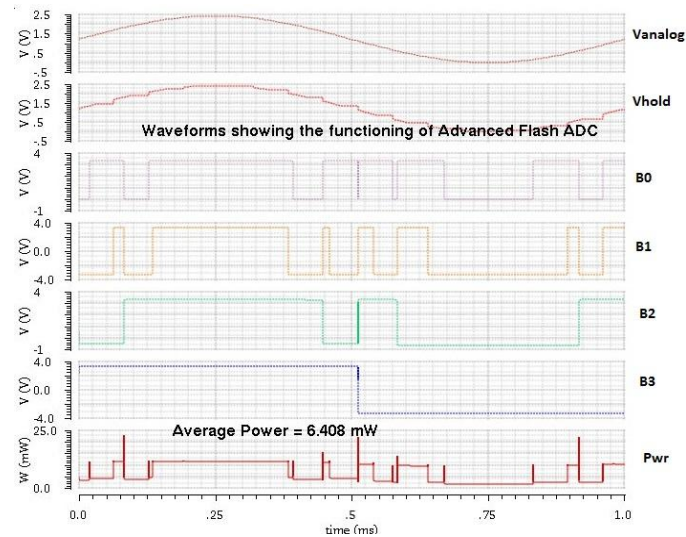


Fig.12. The Simulation results of Flash ADC using multiplexer ($V_{sin} = 1.2V$ at DC 1.2V)

References

- [1]. W. T. Lee, P. H. Huang, Y. Z. Liao, Y. S. Hwang, "A New Low Power Flash ADC using Multiple Selection Method", *Electron Devices and Solid-State Circuits*, pp. 341-344, pp. 1-5, IEEE 2007.
- [2]. M. Suresh, S. Sahu, K. Sadangi, A. K. Panda, "A Novel Flash Analog to Digital Converter Design using Cadence Tool", *International Conference on Advances in Recent Technologies in Communication and Computing*, IEEE 2009.
- [3]. P. V. Kanodiya, A. P. Naik, "Analysis and Design of Flash Analog to Digital Converter for Ultra Wide Band Application", *Engineering (NUICONE)*, pp. 443-447, 2011.
- [4]. S. Rapuano, P. Daponte, E. Balestrieri, L. D. Vito, S. J. Tilden, S. Max, J. Blair, "ADC Parameters and Characteristics", *IEEE Instrumentation & Measurement Magazine* 1094-6969/05©2005 IEEE.
- [5]. R. Megha, P. kumar, "Implementation of Low Power Flash ADC By Reducing Comparators", *Communications and Signal Processing (ICCSP)*, pp. 233-236, 2014.
- [6]. P. Palsodkar, P. Dakhole, A. V. Kale, "Highly Digitalized Flash Analog to Digital (FADC) Converter using Mux Based Decoder Topology", *Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN)*, pp. 1159-1163, vol. 2, 2012.
- [7]. M. F. Snoei, A. J. P. Theuwsen, J. H. Huijsing, K. A. A. Makinwa, "Power and area Efficient Column-Parallel ADC Architectures for CMOS Image Sensors", *Sensors*, pp. 523 – 526, IEEE 2007.
- [8]. J. I. Lee, J. I. Song, "Flash ADC Architecture using Multiplexers to Reduce a Pre-amplifier and Comparator Count", *TENCON 2013*, pp. 1-4, IEEE 2013.
- [9]. L. Nazir, R. N. Mir, "A 4 GS/s, 1.8 V Multiplexer encoder based Flash ADC using TIQ Technique", *Signal Processing and Integrated Networks (SPIN)*, pp. 458-463, IEEE 2014.
- [10]. T. R. Kuphaldt, *Lessons In Electric Circuits*, Volume IV – Digital, Copyright (C) 2000-2014