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A Design of 2*2 Multiplier using 0.18um Technology

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Abstract: Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nano-computing and optical computing. Reversible logic is gaining interest in the recent past due to its less heat dissipating characteristics. There are many arithmetic operations which are performed, on a computer arithmetic unit, through the use of multipliers (e.g., exponential and trigonometric functions). A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Consequently, optimized multipliers are on demand while designing an arithmetic unit. In this paper, a reversible multiplier using reversible gates is proposed. A design of 2*2 multiplier using 180nm technology is successfully synthesized. Cadence Virtuoso 180nm technology is used for the simulation of the design. Multiplier circuit works with 1.8v power supply

Keywords: Reversible logic, Reversible gate, multiplier, Garbage output, Power dissipation.

I. Introduction

In modern VLSI systems power dissipation is very high due to rapid switching of internal signals. A part of this energy loss is due to switches and materials. The primary reasons for the rise in power dissipation are the increase in clock frequency and the increased number of transistors packed onto a chip. The other part arises from Landauer's principle where he proved that in irreversible circuits losing one bit of information dissipates $KT \ln 2$ joules of heat energy, where K is the Boltzmann's constant and T is the absolute temperature [1]. Consider any logic gate (for e.g. AND or OR) with two inputs and one output. On every change of state two bits go in, one bit comes out. Thus there are some resistive losses in the material. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. Furthermore, Bennett showed that reversible circuits do not lose information due to the one-to-one mapping between inputs and outputs; hence no extra energy loss. He showed that reversible computation does not require to erase any bit of information and therefore it does not dissipate any energy for computation [2]. When a computer performs a logical operation, the unwanted bits after the operation are thrown away with sudden changes of voltages from positive to negative, and dissipated as heat. For computer speeds to keep on increasing, we need to 'un-compute' the unwanted bits. On applying reversible computing we can move charges from one node to other with the help of oscillators and switches, hence saving both power and time.

II. Reversible logic

A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. Thus inputs to reversible gates can be uniquely determined from its outputs. A reversible logic gate must have the same number of inputs and outputs. In an n -output reversible gate the output vectors are permutation of the numbers 0 to $2^n - 1$. A reversible gate is balanced, i.e. the outputs are 1's for exactly half of the inputs. Conservative are circuits that have the same number of ones in inputs and outputs. A circuit without constants on its inputs and composed of reversible gates realizes only balanced functions. It can realize non balanced functions only with garbage outputs. Recovering the signal energy to the desired extent is possible using asymptotically adiabatic logic, where the energy is transferred inside the circuit avoiding any abrupt discharge of a high potential to ground.

A. Basic definitions related to reversible logic

Ancilla inputs/constant inputs:

This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.

Garbage outputs:

Additional inputs or outputs can be added so as to make the number of inputs and outputs equal whenever necessary. This also refers to the number of outputs which are not used in the synthesis of a given function. In

certain cases these become mandatory to achieve reversibility. Garbage is the number of outputs added to make an n-input k-output function ((n; k) function) reversible.

We use the words —constant inputs to denote the present value inputs that were added to an (n; k) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs.

Input + constant input = output + garbage.

Quantum cost:

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1.

Flexibility:

Flexibility refers to the universality of a reversible logic gate in realizing more functions.

Gate level:

This refers to the number of levels in the circuit which are required to realize the given logic functions.

Hardware complexity:

This refers to the number of levels in the circuit which are required to realize the given logic functions [12].

B. Features for any gate to become reversible gate as follows[5]:

- Number of input and output lines must be the same.
- Feedback (loop) is not allowed in reversible logic.
- Fan-out is not allowed in reversible logic; Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.
- One of the major constraints in reversible logic is to minimize the number of reversible gates used.
- Minimizing the garbage outputs produced; Garbage output refers to the output that is not used for further computations. Garbage is the number of outputs added to make an n-input k output Boolean function ((n,k)function) reversible.
- Using minimum number of input constants[11].

The following is an example of a reversible gate. Consider the XOR gate; Table I(a) represents its truth table. From this truth table, we can't know the input which gives us 0 output, so it is not one to one mapping. It is not a valid truth table of a reversible gate.

TABLE I. TRUTH TABLE OF REGULAR XOR AND REVERSIBLE XOR GATE

Inputs			Outputs	
A	B		$A \oplus B$	
0	0		0	
0	1		1	
1	0		1	
1	1		0	

(a)

Inputs			Outputs	
A	B	X	$A \oplus B$	
0	0	0	0	
0	1	0	1	
1	0	1	1	
1	1	1	0	

(b)

Table I.(b) represents it by a reversible logic gate. From each output, one can know the corresponding input. X is a garbage output. It is added to make one to one and onto mapping.

III. Reversible Gates

1) NOT Gate

The simplest Reversible gate is NOT gate and is a 1*1 gate. The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Figure 1[13].

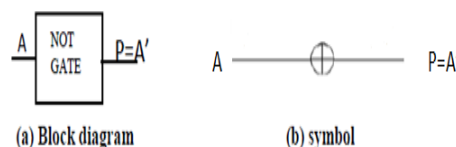


Figure 1: NOT Gate

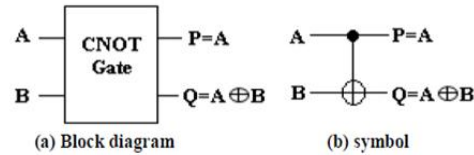
2) CNOT Gate

CNOT gate is also known as controlled-not gate. It is a 2*2 reversible gate. The CNOT gate can be described as:

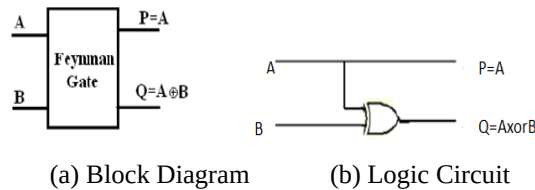
$I_v = (A, B)$; $O_v = (P=A, Q=A \text{ XOR } B)$

I_v and O_v are input and output vectors respectively.

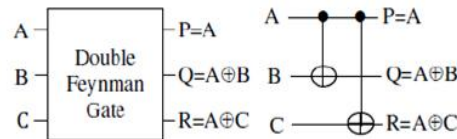
Quantum cost of CNOT gate is 1. Figure 2 shows a 2*2 CNOT gate and its symbol [9].

**Figure 2: CNOT Gate****3) Feynman Gate**

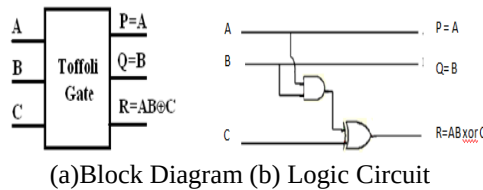
The Feynman gate which is a 2*2 gate and is also called as Controlled NOT and it's widely used for fan-out purposes. The inputs (A, B) and outputs $P=A$, $Q= A \text{ XOR } B$. It has Quantum cost one.

**Figure 3: Feynman Gate****4) Double Feynman gate (F2G)**

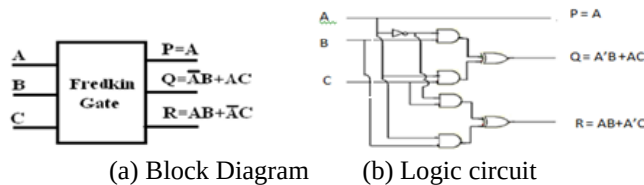
It is a 3*3 Double Feynman gate .The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by $P = A$, $Q=AXORB$, $R=AXORC$. Quantum cost of Double Feynman gate is 2.

**Figure 4: Double Feynman gate****5) Toffoli Gate**

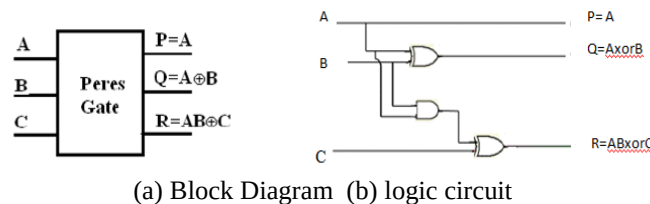
Toffoli gate which is a 3*3 gate with inputs (A, B, C) and outputs $P=A, Q=B, R=AB \text{ XOR } C$. It has Quantum cost five [4].

**Figure 5: Toffoli Gate****6) Fredkin Gate**

Fredkin gate which is a 3*3 gate with inputs (A, B, C) and outputs $P=A, Q=A'B \text{ XOR } AC, R=AB \text{ XOR } A'C$. It has Quantum cost five [3].

**Figure 6: Fredkin Gate****7) Peres Gate**

Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs $P = A; Q = A \text{ XOR } B; R = AB \text{ XOR } C$. It has Quantum cost four [5].

**Figure 7: Peres Gate**

IV. The proposed reversible multiplier

For the sake of simplicity, the proposed reversible multiplier is designed for 2-bit input operands. This can be extended to $n \times n$ bit multiplication. Using the reversible peres gate, 2×2 multiplier can be designed as shown in the figure below. This design requires six peres gates producing 11 garbage outputs. Consider A1, Ao be two bits of a number and B1, Bo be two bits of other number. Let Po, P1, P2, P3 be four output bits of multiplication.

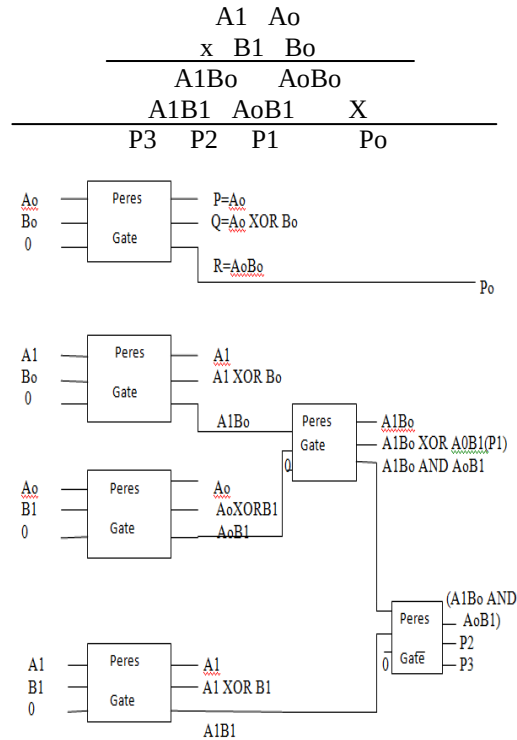


Figure 8: Proposed 2*2 reversible multiplier

Implementation of Peres gate

The reversible peres gate is realized using virtuoso tool of cadence. Spectre simulator of cadence is used to simulate the output. The simulations are performed in 180nm technology. The circuit implementation of peres gate is shown in the figure below.

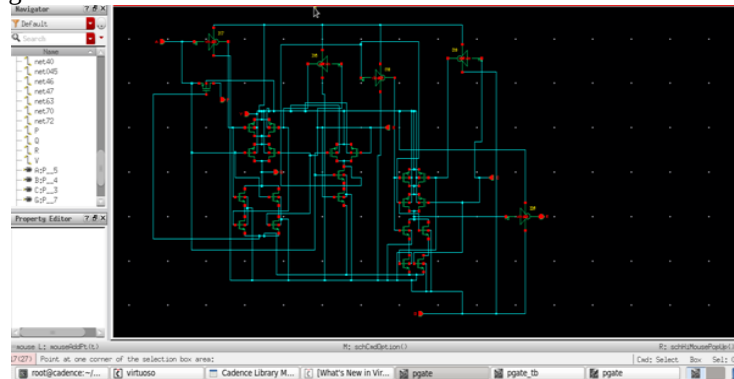


Figure 9: Schematic of Peres gate

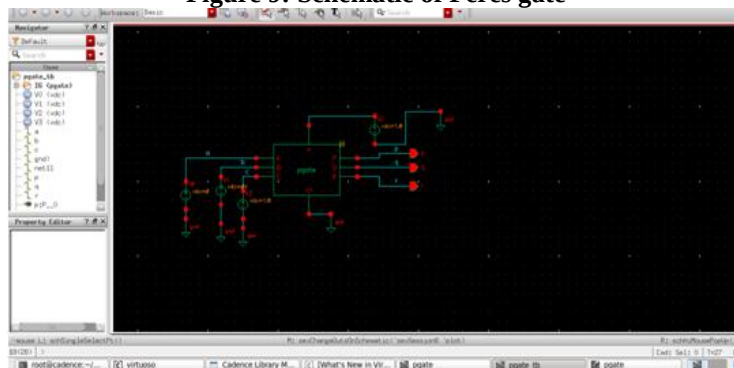


Figure 10: Test bench of peres gate

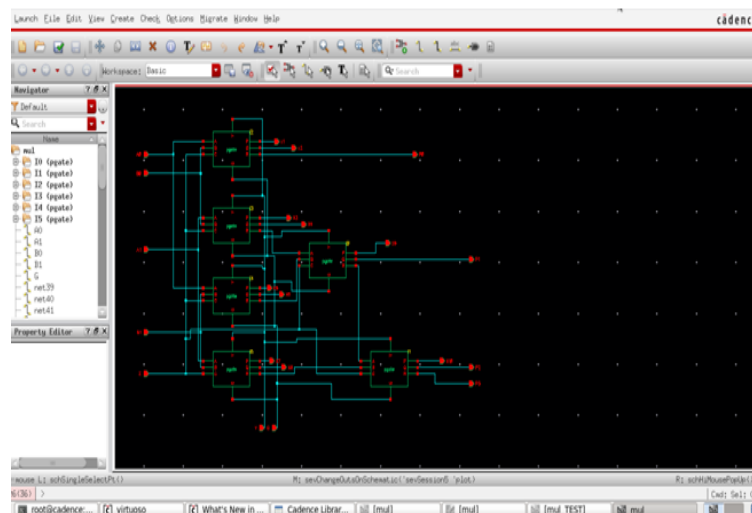


Figure 11: Proposed circuit of multiplier

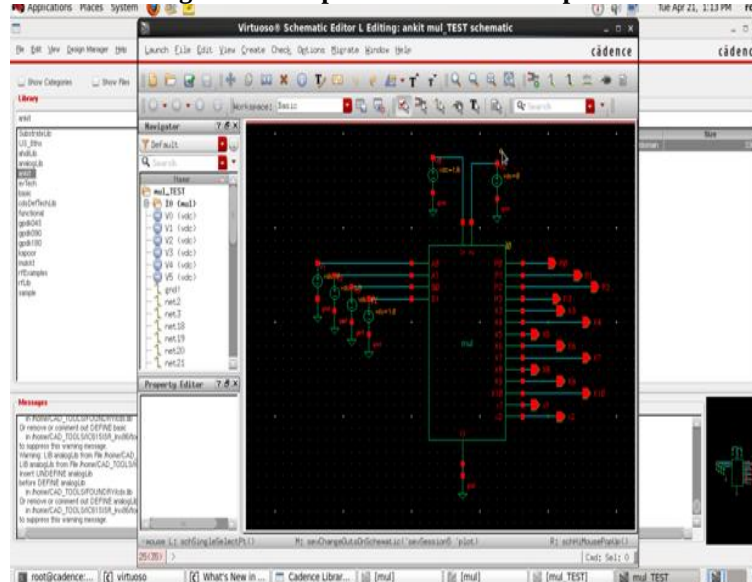


Figure 12: Test bench of multiplier



Figure 13: Output waveforms of multiplier

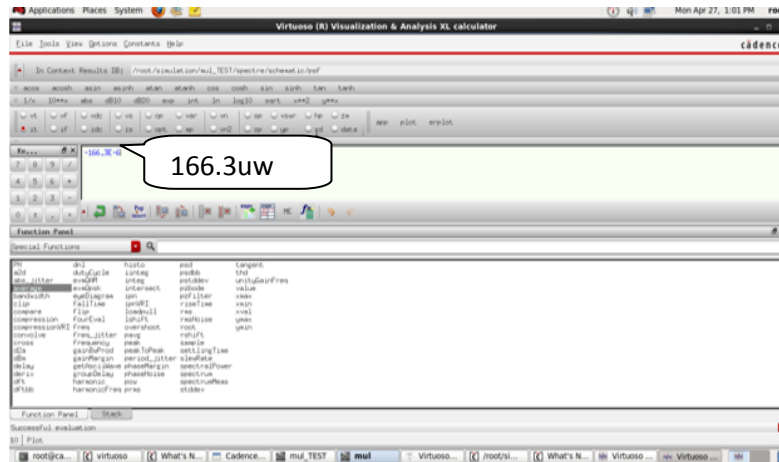


Figure 14: Total power dissipation of multiplier obtained after simulation

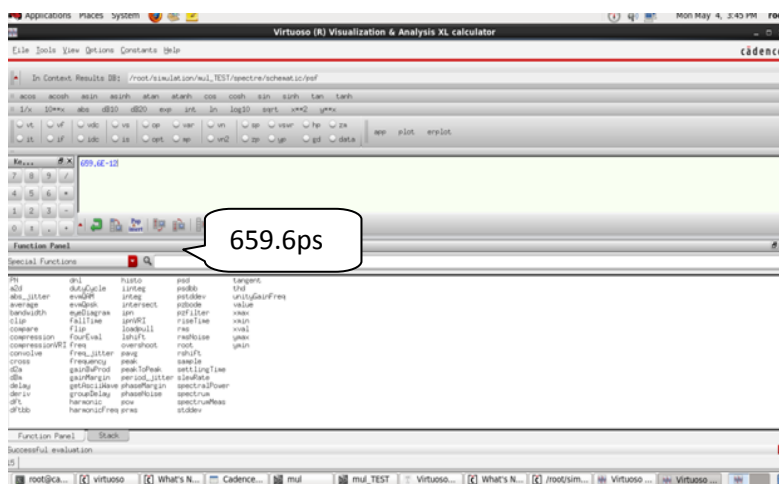


Figure 15: Worst case delay of multiplier circuit obtained after simulation

Table 2. Results of reversible multiplier circuit

Method	Constant inputs	No. of gates	No. of garbage outputs	Power dissipation	Worst case delay
Proposed	6	6	11	166.3uw	659.6psec

V. Scope for future work

The reversible multiplier circuit design which has combined advantages of less power dissipation and timing delay can be used as the building block in the design of arithmetic logic units(ALU's) and other complex arithmetic circuits. The number of garbage outputs, delay, power dissipation of reversible multiplier circuit can be reduced further by improvising the design. The proposed reversible multiplier placement and routing can be carried out by tool like cadence Encounter.

VI. Conclusion

Multiplication is one of the basic functions used in digital signal processing. Most high performance DSP systems rely on hardware multiplication to achieve high data throughput. So it is always desired to design efficient multipliers which consumes less power and gives high speed. This proposed multiplier consumes less power and has less worst case delay. A design of 2*2 reversible multiplier is successfully synthesized. The simulation of the design is done in cadence virtuoso 0.18um technology. The output waveform, power dissipation and worst case delay are shown. Multiplier circuit works with 1.8v supply.

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