



A Modified Power Gating Technique for Ground Bounce Noise Reduction in CMOS Adder Circuit

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Abstract: As technology is continuously scaling down, leakage current is increasing exponentially. Power gating is a very effective technique to reduce the leakage current and leakage power by using sleep transistors to turn off the functional blocks when they are not in use. But when circuit transition goes from sleep to active mode, abrupt transitions introduces Ground Bounce Noise in the circuit which disturbs the normal working of any circuit and tends to give wrong output and also reduces the reliability of circuit. In this paper, we have presented a new power gating technique which uses stacking power gating along with an additional wait mode to reduce ground bounce noise in an adder circuit. A comparison analysis between existing and proposed power gating techniques has been done which shows that the proposed technique reduces leakage by 70.40 and ground bounce noise by 14.02% as compared to existing power gating techniques. We have performed simulations using Cadence Spectre 180nm standard CMOS technology at room temperature with supply voltage of 1V.

Keywords: Ground bounce noise, leakage current, sleep to active mode transition, Sleep Transistors

I. INTRODUCTION

One of the most important issues in VLSI design is leakage current in standby mode with continuous down scaling in advanced CMOS technology. As the dimension of MOSFET is continuously scaling down, the supply voltage and the threshold voltage (V_{th}) of integrated circuits is also scaling down to maintain reliability of devices. Low threshold voltage however leads to an exponential increase in sub-threshold leakage current and hence leakage power [1,2,3]. Power gating is one of the popular leakage power reduction strategies applicable to idle circuits [4]. In power gating technique, high threshold voltage ($high-V_{th}$) sleep transistors (header and footer) are used to cut off the power supply or the ground connection to the idle low threshold voltage ($low-V_{th}$) circuit blocks as shown in figure 1.

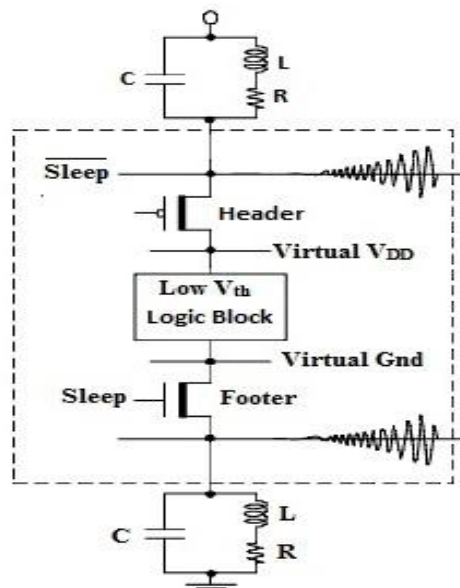


Figure 1 Power and Ground bounce noise generated in Conventional CMOS circuit

While operating the circuit in the *active* mode, the sleep transistor is turned on to perform the desired functionality of the circuit. In the *sleep* mode, the sleep transistor is turned off, due to which the source nodes of the transistors in the functional block float, thus cutting off the leakage path to the ground. The only path that is left for the leakage current to flow is the parasitic capacitances of the transistor shown in Figure 2. Thus the leakage current starts charging up the parasitic capacitances of the transistors. When the circuit is turned on, these capacitances need to be discharged to get the circuit back to the normal mode of operation. This sudden

discharge of current causes voltage fluctuations in the circuit. This sudden voltage fluctuation is known as Ground Bounce Noise [5]. This ground bounce might cause performance degradation or even worse, functional failures in the adjacent units. Transistors may stuck into a meta-stable state causing failure of the circuit operation and it can results in increase of power dissipation and leakage current [6].

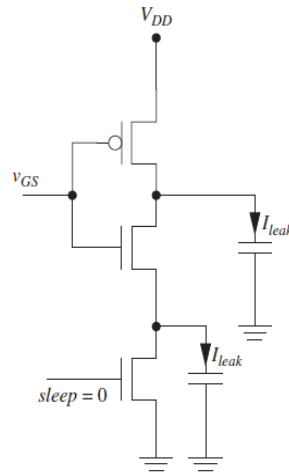


Figure 2 Parasitic capacitances in a inverter circuit being charged up by the leakage current when the sleep transistor is off.

Ground bouncing phenomenon in CMOS 1-bit adder circuit is evaluated in this paper as adders are heart of computational circuits and many complex arithmetic circuits are based on the addition, this is why building low leakage adder cells are of great interest. A novel stacking power gating with additional wait mode structure is presented in this paper to effectively suppress the ground bouncing noise during mode transition (sleep to active mode transition) and leakage current during standby mode in adder circuits. The remainder of this paper is organized as follows. In section II, full adder circuit with stacking power gating technique and its equivalent circuits are discussed. In section III, analysis of the stacking power gating technique with wait mode has been done and its equivalent circuit is explained. In section IV simulation results of conventional CMOS full adder cell and full adder cell with stacking power gating circuits are explained. Then the paper is summarized in section V.

II. PROPOSED STACKING POWER GATING TECHNIQUE WITH WAIT MODE

Stacking power gating technique with wait mode (shown in Fig. 3) has been introduced in this section to further reduce the activation noise and standby leakage current. In this technique high threshold sleep transistors (N_1 , N_2 and P_1) are used to reduce leakage current effectively. Transistor stacking is an effective way to reduce leakage current so two high threshold NMOS transistors (N_1 and N_2) are used in stack. An additional wait mode is being introduced between sleep and active mode so that discharging of virtual ground voltage (V_{GND1}) during sleep to active mode can be divided into two parts using wait mode which will reduce peak of ground bounce noise efficiently. Delay ΔT is provided between the activation of two transistors (N_1 and N_2). This delay isolates the ground for a short period of time during the mode transition. An additional capacitor C_2 is inserted in the intermediate node V_{GND2} to control the drain current flowing through the second sleep transistor N_2 in mode transition. Forward body biasing voltage (V_{bias}) has been applied to wait transistor so that more virtual ground voltage get discharged during sleep to wait mode transition. Detailed analysis has been done in Section III.

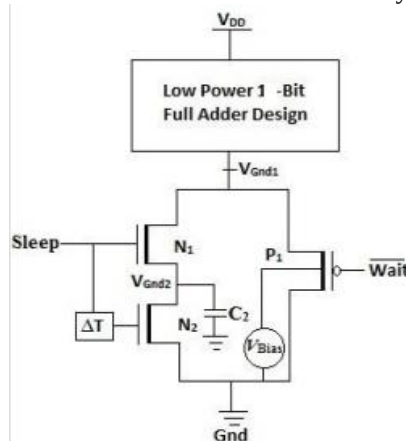


Figure 3 Stacking Power gating with wait mode

III. ANALYSIS OF STACKING POWER GATING TECHNIQUE WITH WAIT MODE

This power gating technique works on two strategies: (A) Strategy for standby leakage current reduction and (B) Reduction of Ground bounce noise (GBN) during mode transition.

A. Strategy for Standby Leakage Current Reduction

In this technique the leakage current is reduced by turning OFF the transistors N_1, N_2 and P_1 in standby mode. The expression for the sub threshold leakage current is [3]

$$I_{sub} = A e^{\frac{q}{n k T} (V_{gs} - V_{th0} + \gamma V_{bs} + \eta V_{ds})} \left(1 - e^{\frac{-q V_{ds}}{k T}}\right)$$

$$A = \mu_n C_{ox} \frac{W}{L} \left(\frac{k T}{q}\right)^2 e^{1.8} \quad (1)$$

Where V_{th0} is the zero bias threshold voltage, γ is the body effect coefficient and η is the DIBL coefficient, C_{ox} is the gateoxide capacitance and μ_n is mobility. V_{gs} , V_{bs} and V_{ds} are the gate to source, bulk to source and drain to source voltages respectively. Equation (1) shows that the sub threshold leakage current will reduce exponentially if body effect is increased (negative V_{bs}) and drain-to-source voltage V_{ds} is decreased. The stacking structure [7] is shown in Fig. 4. When sleep transistors are turned OFF in standby mode then the voltage of the intermediate node V_{GND2} raises to the positive values due to small drain current of the sleep transistor N_1 . Further, due to this positive potential at the intermediate node the drain-to-source potential (V_{ds}) of N_1 decreases which results in negative body-to source potential (V_{bs}) of N_1 causes more body effect. This will reduce leakage current effectively.

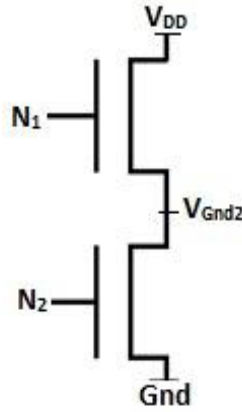


Figure 4 Stacking Power Gating

B. Strategy to Reduce Peak of Ground Bounce noise During Mode transition

Ground bounce noise can be reduced by limiting the large transient current flowing through the sleep transistors during mode transition. When sleep transistor is turned ON, voltage of virtual ground goes down sharply which causes fluctuations in ground rail. The voltage of the virtual ground line is maintained at V_{DD} during the sleep mode. Before the activation of the circuit, the P_1 transistor is turned on while transistor N_1 and N_2 is maintained in cut-off. In this situation the circuit transits to the intermediate wait mode. Body biasing has been done for wait transistor so that threshold voltage of wait transistor can be reduced without increasing the width and more virtual ground voltage can discharge during transition from sleep to wait mode [8]. The virtual ground line is discharged to the threshold voltage of the wait transistor V_{tp} and then transition from wait mode to active mode takes place. Due to two-step transitions from the sleep mode to active mode through wait mode voltage swings on ground rail get suppressed which leads to ground bounce noise suppression [9,10]. To complete the reactivation process from wait to active mode, the stacked transistors N_1 and N_2 are subsequently turned on. The transistor P_1 is turned off. By isolating the ground for small duration during mode transition and turning ON the N_1 transistor in linear region instead of saturation region ground bounce noise will reduce effectively. During wait to active mode transition, transistor N_1 is turned ON and transistor N_2 is turned ON after a small duration of time (ΔT). The logic circuit is isolated from the ground for a short duration as the transistor N_2 is turned OFF. During this time, the ground bounce noise can be greatly reduced by controlling the intermediate node voltage V_{GND2} and operating the transistor N_1 in triode region. The intermediate node (V_{GND2}) voltage can be controlled by (1) Inserting proper amount of delay, that is less than the discharging time of the N_1 transistor, and (2) Proper selection of the capacitance C_2 .

Since the voltage across the capacitor does not change instantaneously, the voltage across capacitors C_1 and C_2 remain same by instantaneously turning on the sleep transistor N_1 . Now the equivalent circuit for stacked transistors during wait to active mode is shown in Fig. 5.

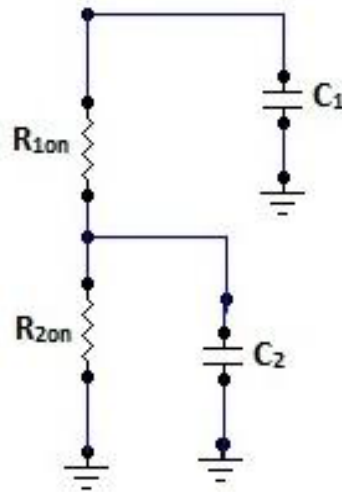


Figure 5 Equivalent circuit of stacking sleep transistors during wait to active mode transition

Here R_{1on} is the ON resistance of sleep transistor N_1 , C_1 is the internal capacitance at virtual ground node V_{GND1} and C_2 is the external capacitance at intermediate node V_{GND2} . The voltage across the capacitor $C_1 \approx V_1$, and the voltage across the capacitor $C_2 \approx V_2$. When $\Delta T > t > 0$, the capacitor C_1 having voltage V_1 will begin to discharge, and the capacitor C_2 will be charging by the amount with which C_1 is discharging. This process will continue until both the capacitances have the same potential. From above point of view by controlling the capacitor C_2 and ΔT we will be able to control the intermediate node voltage V_{GND2} so that both the transistors (N_1 and N_2) can be turned on in triode region and hence voltage swing at ground rail during wait to active mode transition can be controlled and ground bounce noise will reduce effectively.

IV. RESULTS AND DISCUSSIONS

In this section, we have performed simulation of our conventional 28 T and modified 28T adder (adder with stacking power gating technique) on Cadence Virtuoso Tool and SPECTRE Simulator at 180 nm Technology.

A. Active Power

The Active power is dissipated by the circuit when the circuit is operation state. Here we will calculate the active power of the circuit at basic of voltage and temperature for the 180 nm technology. The Active power consumption of CMOS circuit is consumed by the following equation.

$$P_{active} = P_{dynamic} + P_{static} \quad (2)$$

$$= P_{switch} + P_{short} + P_{leak}$$

$$P = F_C V_{DD} + I_{short} V_{DD} + I_{leak} V_{DD} \quad (3)$$

Where F_C = Clock frequency, V_{DD} = Power supply, I_{short} = Short circuit current, I_{leak} = Leakage current.

As shown the table I, in the case of modified 28T adder with stacking power gating active power is reduced as compared to conventional 28T adder. The reduction is almost 44% at voltage 1.8 V and temperature 27°C.

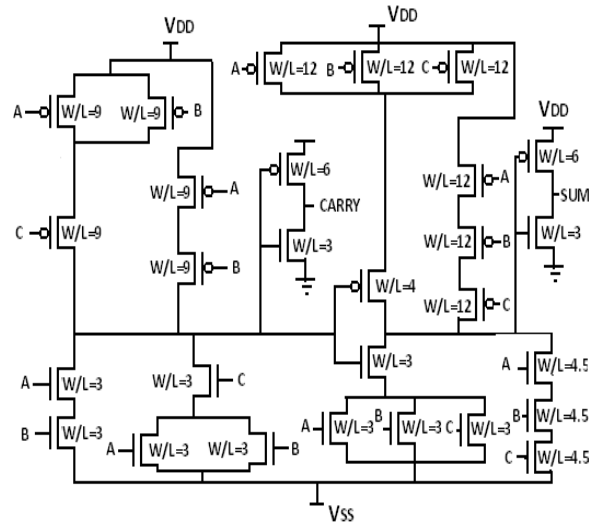
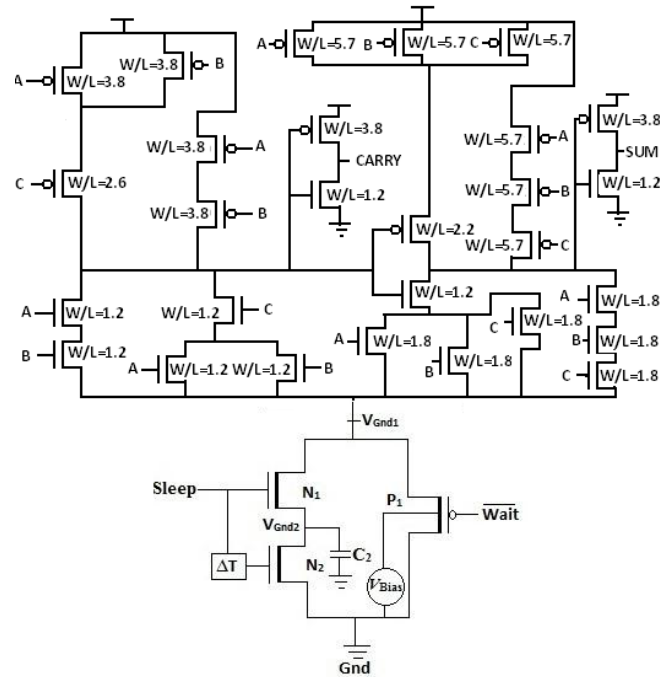


Figure 6 Conventional 28T adder circuit

Table I Active Power Dissipation of 28T Adder

Circuit	Conventional Adder(nW)	Modified adder(nW)
	1.8V,27°C	1.8V,27°C
Active Power	108.67	61.84

**Figure 7 Modified Adder circuit****B. Stand By Leakage Current**

The stand by leakage is obtained when the circuit in idle mode. When we measure the leakage current in stacking power gating then both sleep transistors are off. The basic equation of stand by leakage is [11]:

$$I_{leak} = I_{sub} + I_{ox} \quad (4)$$

Where, I_{sub} = Subthreshold leakage current, I_{ox} = Gate oxide current

Stand by leakage current is measured by at 1.8V and 27 °C. It is greatly reduced almost 80% in modified 28 T adder with stacking power gating .The table II shows the leakage current at various voltage and various temperature .

C. Leakage Power

The stand by leakage power is measured at the time of idle mode. Here measured the leakage power when the sleep transistor is off. Basically the stand by leakage power is the product of the leakage current and supply voltage [12]. The basic equation of leakage power is

$$P_{leak} = I_{leak} V_{DD} \quad (5)$$

Table II The stand by Leakage Current and power due to Voltage variation

Voltage (V)	Leakage Current(nA)		Leakage power(nW)	
	Conv. Adder	Modified Adder	Conv. Adder	Modified Adder
0.7	31.8	4.3	36.9	17.7
1.0	53.7	18.8	79.4	41.1
1.5	76.8	43.7	101.5	69.3
1.8	102.6	54.9	133.8	98.2

Table III The stand by Leakage Current and power due to Temperature variation

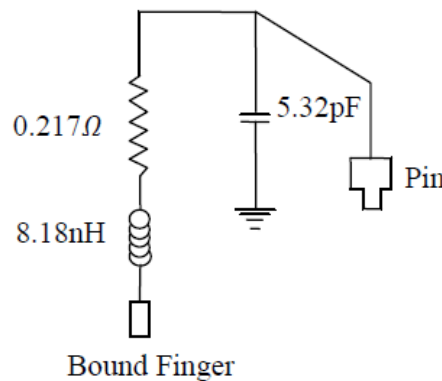
Temp. (°C.)	Leakage Current(nA)		Leakage Power(nW)	
	Conv. Adder	Modified Adder	Conv. Adder	Modified Adder
27	102.6	54.9	133.8	98.2
47	103.1	65.7	135.7	126.7
67	103.7	69.1	139.4	139.4
87	104.2	77.8	143.5	152.3

The table II and table III shows leakage power is reduced almost 30% in various voltages and temperatures after applying stacking power gating.

D. Ground Bounce Noise

During mode transition of the circuit an instant current pass from sleep transistor, which operates in saturation region at that time and causes a sudden flow of the current. Because of self inductance of the off- chip bonding wires and parasitic inductance on chip power rails , results an increase in voltage level in the circuits ground rail depends on input / output buffers and internal circuitry[13]. The noise depends on the voltage. All the below mentioned results have been simulated under the condition that the all logical inputs of full adder circuit are held at logic 1 for ground bounce noise calculation (worst case for peak ground bounce noise).The ground bounce noise model [14] is shown in Fig.8.

As shown in the Table IV & V the ground bounce noise is reduced up to 90 % in to various voltage and temperature. The ground bounce noise is measured at 1.8V and 27°C. It is greatly reduced almost 90 % in modified 28T adder with stacking power gating and also shown in the table IV & V at various voltage and various temperature. As sleep input is given to transistor N_2 after a delay ΔT , so peak of ground bounce noise also vary with respect to ΔT Variation in Ground Bounce Noise with respect to delay ΔT is shown in figure 9.

**Figure 8 DIP-40 package pin ground bounce noise mode****Table IV Ground Bounce Noise for 28T Adder**

Voltage (V)	Ground Bounce Noise	
	Conventional (uV)	Modified (uV)
0.7	9.7	0.39
1.0	19.5	0.97
1.5	27.3	1.7
1.8	34.6	4.1

Table V Ground Bounce Noise for 28T Adder

Temperature (°C.)	Ground Bounce Noise	
	Conventional (uV)	Modified (uV)
27	34.6	4.1
47	45.7	5.7
67	59.1	6.3
87	67.8	6.9

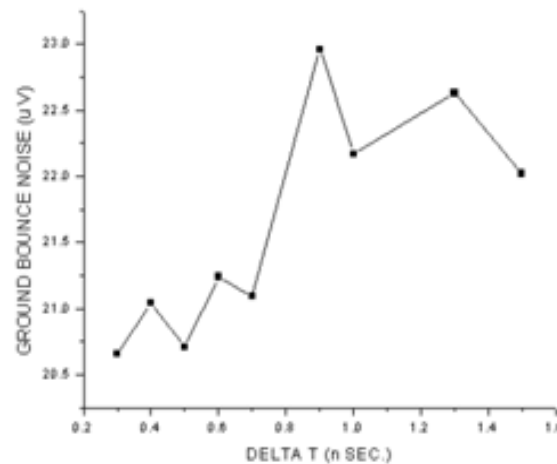


Figure 9 Variation of Ground Bounce Noise with respect to ΔT

V. CONCLUSION

In this paper we proposed a modified 28T Adder for arithmetic logic circuits with low ground bounce noise and reduce leakage power. Here we have used high performance power gating technique to reduced active power, leakage power, leakage current and ground bounce noise. The leakage current up to 80% and leakage power up to 30%. The ground bounce noise is reduced to up to 90% and active power is reduced up to 44 %.The proposed modified 28T adder is operated at various voltages and various temperatures.

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