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Design a 5T SRAM by using self controllable voltage level leakage reduction technique with CMOS Technology

Laxmi Singh¹, Ajay Somkuwar²

¹Department of Electronics & Communication, Corporate college of Technology, Bhopal, INDIA.

²Department of Electronics & Communication Bhopal, MP, INDIA

Abstract: The combination of complexity and speed, most of the application in VLSI system. The integrated circuit memories are essential elements for digital and analog circuit. High performance and cost effective circuits implement by using a CMOS Technology. Here we implemented a 5T SRAM (static random access memory) by using a self controllable voltage level (SVL) technique. The SVL technique is low leakage power reduction technique in which has upper SVL and lower SVL is used. The simulation is done by using a MICROWIND 3.1 and DSCH2 with SVL technique. Using a 0.12 μ m technology with DRC rule checker check the designing of the circuit. By this technique give a 98% advantage of reducing a leakage power. In the field of power reduction also give advantage.

Keywords- self controllable voltage level technique, low dynamic power consumption, leakage power, and high performance, less area.

I. Introduction

Semiconductor memory arrays capable of storing big quantities of digital information are vital to all digital systems. The amount of memory necessary in a particular system depends on the type of application. The growing demand for larger data storage capacity has determined the fabrication technology and memory development towards more compact design rules and consequently, toward higher data storage densities. The maximum achievable data storage capacity of single-chip semiconductor memory arrays approximately increases. On-chip memory arrays have become widely used.

The higher memory density and larger storage capacity will go on with to drive the important edge of digital system design. The number of stored data bits per unit area determines the overall storage. The memory access time is the time required to store and read a particular data bit in the memory array. The access time determines the memory speed. It's an important performance criterion of the memory array. Finally, the static and dynamic power consumption of the memory array is a major factor to be measured in the design because of the increasing importance of low-power applications.

In this research paper design a 5T SRAM by using a self controllable voltage level technique. Basically it's a leakage current reduction technique. By using this power consumption is also reduced.

SRAM is static random access memory in which used a 5 transistor to perform a read and write operation. It's a volatile in nature. To access a particular memory cell a 5T SRAM, the bit line and the word line must be activated. Once a memory cells are selected a data read and a data write operation have performed.

II. History of Work

The number of investigation is defined by a history of work in such manner like a Top down pass transistor logic is used in research paper [1]. Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits are presented in [2]. Ultra Low Power Full Adder Topologies have defined in [3]. Novel Low Power Full Adder Cells in 180nm CMOS Technology have investigated in [4]. Gate Leakage Reduction for Scaled Devices Using Transistor Stacking is presented in [5]. Impact of technology scaling on CMOS logic styles gives in [6]. Leakage power analysis and comparison of deep submicron logic gates idea give in these [7]. The idea about the Low-power CMOS digital design shows in [8]. Low-power logic styles CMOS versus pass-transistor logic are presented in [9]. The idea related to Principles Of Cmos Vlsi Design have find in [10]

III. Proposed Work

The read-write (R/W) memory circuits are designed to permit the writing and reading of data bits to be stored in the memory array. The memory circuit is said to be static if the stored data can be retained as long as a sufficient power supply voltage is provided without any need for a periodic refresh operation. The data storage cell or in

other word the 1-bit memory cell in static Random access memory consists of a simple latch circuit with two stable operating states. Depending on the conserved state of the two-inverter latch circuit, the data being held in the memory cell will be interpreted either as logic "0" or as logic "1." To access the data contained in the memory cell via the bit line, we need at least one switch, which is controlled by the corresponding word line, two complementary access switches consist of nMOS pass transistors are implemented to connect the 1-bit SRAM cell.

The five -transistor SRAM cell can be implemented by using a polysilicon and n+ diffusion layer and p+ diffusion layer and metal layer. The two stable operating points of this basic latch circuit are used to store a one-bit piece of information. The pair of cross-coupled inverters make up the central component of the SRAM cell. To perform read and write operations. We use one nMOS pass transistors which driven the by the word line signal. the memory cell by raising its word line voltage to logic "1," hence, the pass transistors M3 is turned on. Once the memory cell is selected, four basic operations may be performed on this cell.

Figure 1 shows the schematic of 5T SRAM in which used a three NMOS and two PMOS transistor. Which transistor is connected to word line are called access transistor. With the help of these transistor controlling the bistable circuitry of SRAM. When bit line is activated and word line is low, no operation is performed by the circuit. When raising the word line of 5T SRAM the read and write operation is performed. Bit line basically a information.

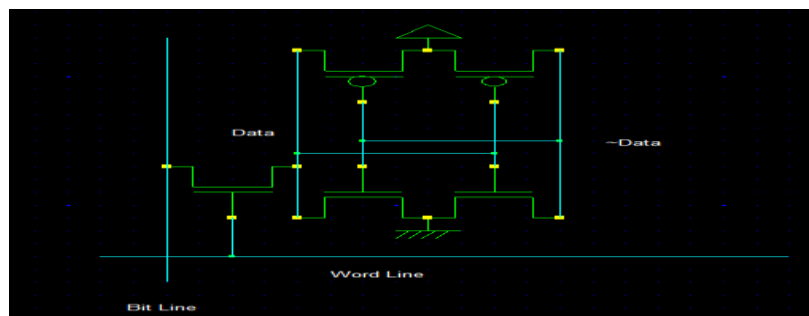


Figure 1. Schematic of 5T SRAM

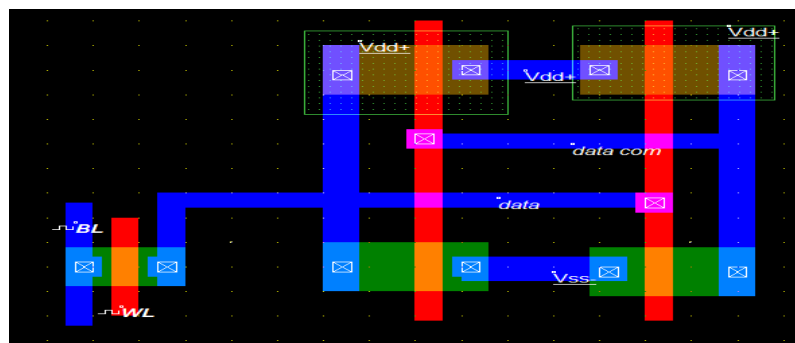


Figure 2. Layout of 5T SRAM

The layout diagram of 5T SRAM shown in figure 2 in which used a polysilicon, n+ diffusion, p+ diffusion and metals for interconnection and for supply used a VDD and for ground used a GND. Gate connection is made by the polysilicon and source and drain connection is made by the contact of n+ diffusion layer and p+ diffusion layer. Word line signal given to the polysilicon and bit line signal given to the metal layer with source connection.

Figure 3 shows a simulation of 5T SRAM in which shows a voltage versus time waveform. When the bit line is high and in that time word line is also high then output is high otherwise its low.

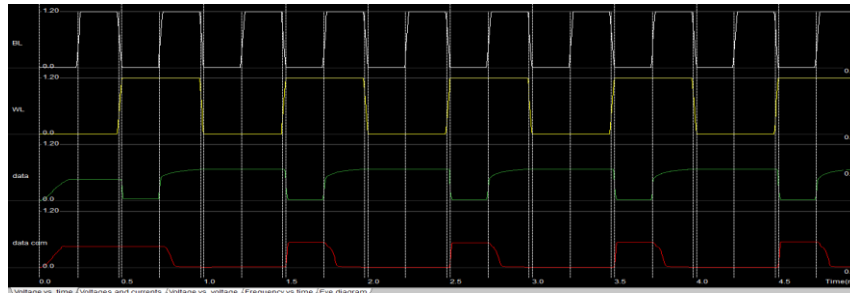


Figure 3. Voltage vs. time waveform

Figure 4 shows the voltage versus current waveform in which shows the leakage current around a 0.062ma and dynamic power consumption is 18.061μw.

The stand by Power dissipation of the SRAM cell is

$$P_{stand-by} = V_{DD} \cdot \frac{\mu_n C_{ox}}{2} \cdot \left(\frac{W}{L} \right)_{load} \cdot |V_{T,load}|^2 \quad \text{----- (1)}$$

Here

VDD = Power supply voltage

μn = mobility of electron

Cox = capacitance for silicon dioxide

VT = Threshold voltage

W = Width

L = length

Now the circuit is implemented by using a self controllable voltage level technique. In self controllable voltage level technique is divided into two categories first is upper self controllable voltage level and second is lower self controllable voltage level technique.

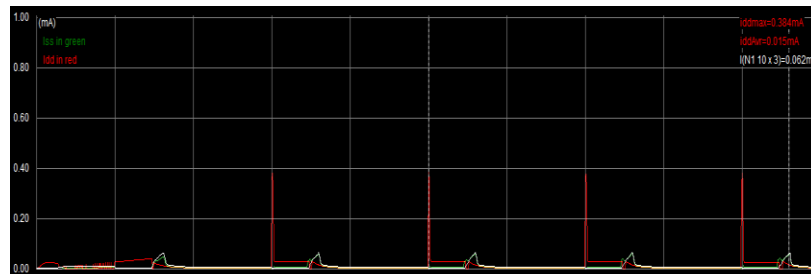


Figure 4. Voltage vs. current waveform

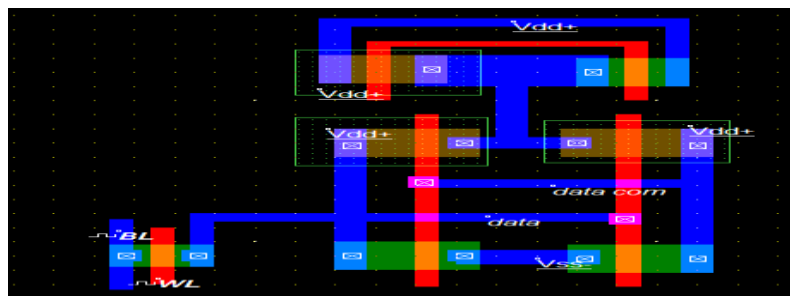


Figure 5. Layout of 5T SRAM with upper SVL

The upper self controllable voltage level technique uses a one NMOS and one PMOS. Connection of NMOS and PMOS like a polysilicon is connected together means that the gate of both MOS connected together. One part of the metal is connected to the VDD and other part is connected to the circuit. This connection is shown in figure 5 in which top part shows a upper SVL and bottom part shows a 5T SRAM circuit.

Now the lower self controllable voltage level is connected to the lower part of the circuit shown in figure 6. In which one part of the metal is connected to the VSS and other part is connected to the circuit.

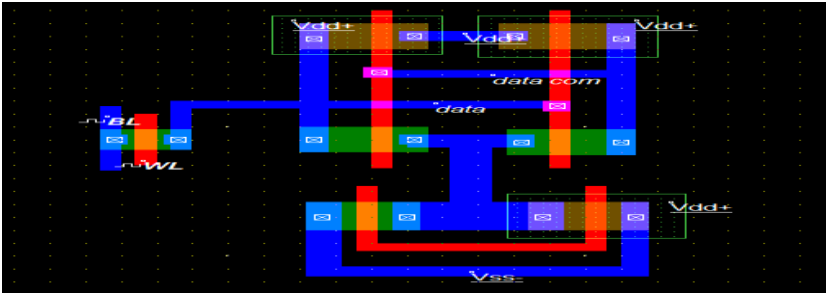


Figure 6. Layout of 5T SRAM with lower SVL

Now the combination of upper self controllable voltage level (SVL) and lower self controllable voltage level (SVL) Shown in figure 7. The simulation of 5T SRAM with self controllable voltage level is shown in figure 8. To implement with SVL technique leakage current is 0.001ma. the leakage power is reduced up to a 98%.

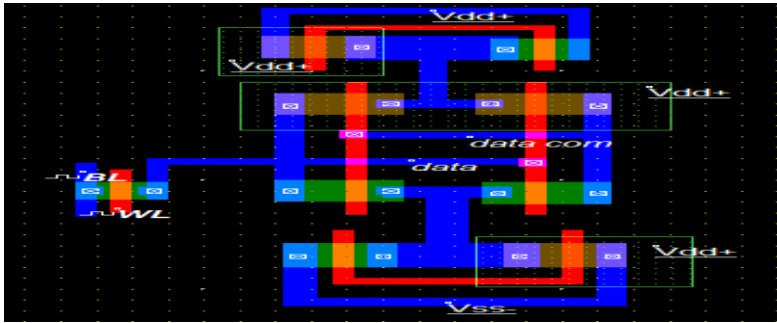


Figure .7 layout of 5T SRAM with SVL technique

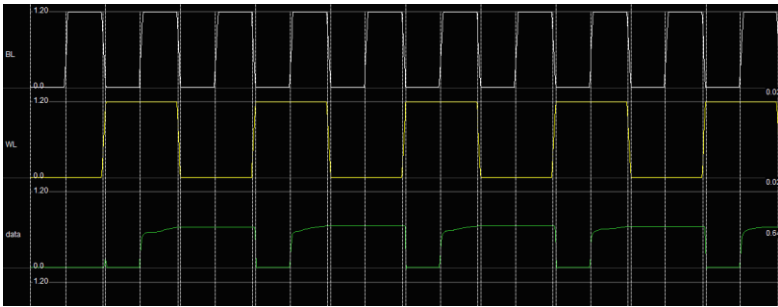


Figure 8. Voltage vs. time of 5T SRAM with SVL technique

IV. Circuit Simulation Result

To simulate a circuit using a MICROWIND 3.1 and DSCH2 with the 1.2VDD and 27°C temperature. In designing we have to use polysilicon and n+ diffusion and p+ diffusion and some metals for interconnection . check the layout by using a design rule checker. In table –I shows a parameter of 5T SRAM. Table –II shows a simulation result of SVL based 5T SRAM.

TABLE –I
PARAMETER OF 5T SRAM

Process technology	0.12µm
Power supply voltage	1.2v
Pre charge voltage	1v

TABLE –II
SIMULATION RESULT OF SVL BASED 5T SRAM

Circuit	Leakage current
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5T SRAM during write operation	0.062ma
5T SRAM with SVL	0.001ma

V. Conclusions

In this research paper we presented a 5T SRAM with self controllable voltage level technique. The circuit structure and layout of Simulation is done by using a microwind 3.1 and DSCH 2. To implement 5T SRAM with self controllable voltage level gives the advantageous of reduction up to 98%. VDD is used in this 1.2V and precharge voltage is 1V. Here 0.12 μ m technology is used.

VI. References

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