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Design of Control Unit for Low Power ALU with a Barrel Shifter Using Reversible Logic

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Abstract: Reversible Logic is becoming more and more prominent special optimization technique having its applications in Low Power CMOS designs, Quantum Computing and Nanotechnology. ALU is a fundamental building block of a central processing unit (CPU) in any computing system. Reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized. In this paper, as a part of ALU design, a Reversible low power control unit for arithmetic operations is proposed.

Keywords: Reversible logic circuit, reversible logic gates, Reversible arithmetic logic unit, barrel shifter, quantum computing, nanotechnology based systems.

I. Introduction

Irreversible hardware computation results in power dissipation due to information loss. As demonstrated by R.Landauer in the early 1960s, irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss. According to his research, the combinational logic circuits dissipate heat in an order of $kT \ln 2$ joules of energy for every bit of information that is erased, where $k=1.3806505 \times 10^{-23}$ m² kg-2k⁻¹ (joules Kelvin⁻¹) is the Boltzmann constant and T is the operating temperature. For room temperature T the amount of dissipating heat is small (i.e. 2.9×10^{-21} joule), but not negligible. The design that does not result in information loss is called reversible. It naturally takes care of heating generated due to the information loss. Such gates or circuits allow the Reproduction of the inputs from observed outputs and we can determine the inputs from the outputs. Thus reversibility will become an essential property in future circuit design. Reversible logic has applications in various research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology. The difference of reversible logic synthesis compared to binary logic synthesis can be summarized as follows:

- 1) The gates used to implement the circuit have the equal number of inputs and outputs.
- 2) Every output of a gate, which is not used in the circuit, is a garbage signal. A good synthesis method minimizes the number of garbage signals.
- 3) The total number of constants at inputs of the gates is kept as low as possible.
- 4) A gate output can be used only once (the fan-out count of each output is equal to one). If two copies of a Signal are required, a copying circuit is used.
- 5) The resulting circuit is acyclic.

In this paper, as a part of ALU design, a Reversible low power control unit for arithmetic operations is proposed by using different types of reversible gate such as MTSG, TG, FRG and Peres Gate.

II. Reversible Logic

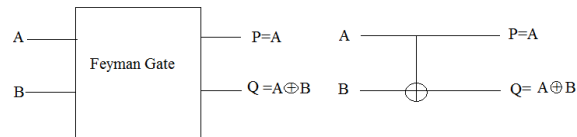
The n- input and k- output Boolean function $f(x_1, x_2, x_3, \dots, x_n)$ (referred to as (n,k) function) is called reversible if :

- 1) The number of outputs is equal to the number of inputs and
- 2) Each input pattern maps to unique output patterns [13]

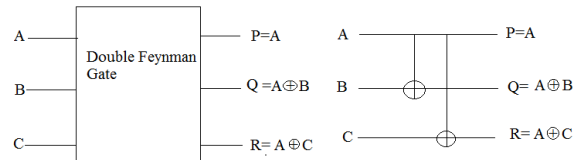
In other words, reversible functions are those that perform permutations of the set of input vectors.

III. Reversible Logic Gates

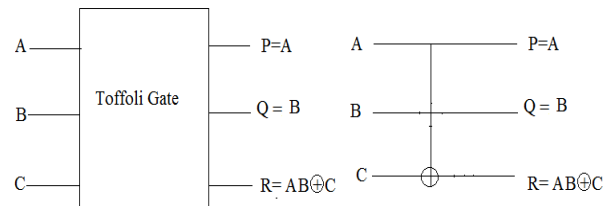
Feynman gate: It is a 2*2 Feynman gate [6]. The input vector is I (A, B) and the output vector is O(P, Q). The outputs are defined by $P=A$, $Q=A \oplus B$. Quantum cost of a Feynman gate is 1.



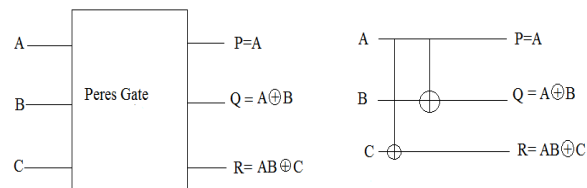
Double Feynman gate: It is a 3*3 Double Feynman gate [6]. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The outputs are defined by $P = A$, $Q = A \oplus B$, $R = A \oplus C$. Quantum cost of double Feynman gate is 2.



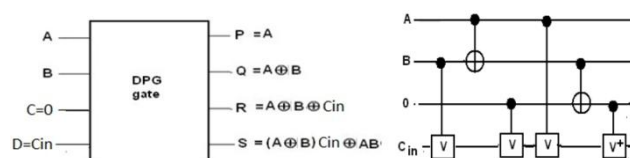
Toffoli gate: It is a 3*3 Toffoli gate [7]. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The outputs are defined by $P = A$, $Q = B$, $R = AB \oplus C$. Quantum cost of a Toffoli gate is 5.



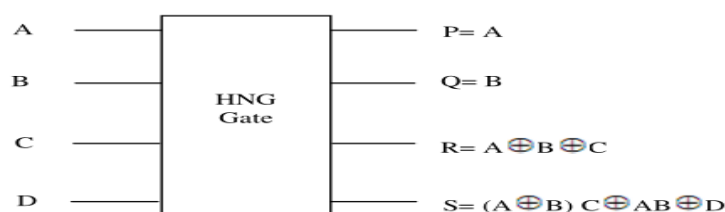
Peres gate: It is a 3*3 Peres gate [11]. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The output is defined by $P = A$, $Q = A \oplus B$ and $R = AB \oplus C$. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.



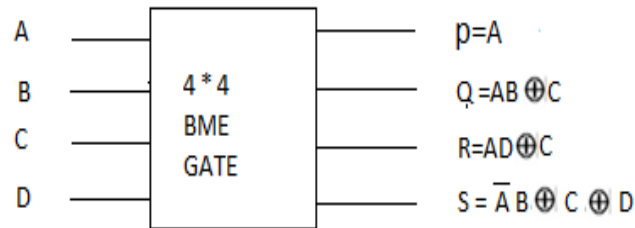
DPG gate: It is a 4*4 DPG gate [25]. The input vector is $I(A, B, C, D)$ and the output vector is $O(P, Q, R, S)$. The quantum cost of DPG gate as full adder is 6.



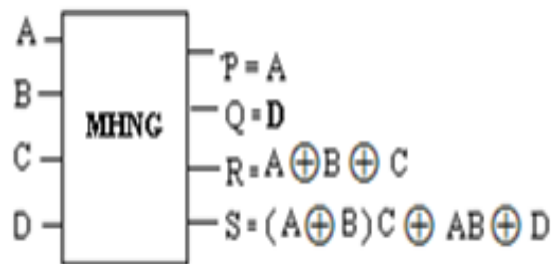
HNG Gate: It is a HNG Gate [9]. The input vector is $I(A, B, C, D)$ and the output vector is $O(P, Q, R, S)$. $P = A$, $Q = B$, $R = A \oplus B \oplus C$ and $S = (A \oplus B) \oplus C \oplus AB \oplus D$. The full adder using HNG is obtained with $C = Cin$ and $aD = 0$.



BME gate : It is a 4*4 reversible logic gate named BME gate[26]. The input vector is I (A,B,C,D) and the output vector is O(P,Q,R,S).The output is defined by $P=A$, $Q=AB \oplus C$, $R=AD \oplus C$ and $S= \bar{A}B \oplus C \oplus D$. The Quantum Cost of BME gate is 5.



MHNG gate : It is a MHNG gate[27].The input vectors is I(A,B,C,D) and the output vectors is O(P,Q,R,S).



IV. Proposed Arithmetic Logic Unit with a Barrel Shifter

A barrel shifter is one form of combinational circuit that shift or rotates the input data bits by the number of bits positions specified by a binary value on a set of selection lines.

- 1) When $S_3=0$, no shifts operation is occurs and the input data has a direct path to the outputs.
- 2) When $S_3=1$, the input data is rotated one position, with B going to R0 and A going to R1 position.

Four control variables S_3, S_2, S_1, S_0 along with C_{in} select twelve different arithmetic–logic operations and shift operation and S_3, S_2 distinguishes between shift and arithmetic-logic operation.

When $S_3=0$ and $S_2=0$ then Arithmetic operations are performed.

- 1) When $S_3=0$ and $S_2=1$ then logic operations are performed.
- 2) When $S_3=1$ then shift operation is performed.

Fig I Shows the functional block of how the barrel shifter works with ALU.

Function Select					Output Equals	Function
S_3	S_2	S_1	S_0	C_{in}		
0	0	0	0	0	$F=A$	Transfer A
0	0	0	0	1	$F=A+1$	Increment A
0	0	0	1	0	$F=A+B$	Addition
0	0	0	1	1	$F=A+B+1$	Addition with borrow
0	0	1	0	0	$F=A-B-1$	Subtraction with borrow
0	0	1	0	1	$F=A-B$	Subtraction
0	0	1	1	0	$F=A-1$	Decrement A
0	0	1	1	1	$F=A$	Transfer A
0	1	0	0	x	$F=A \vee B$	OR
0	1	0	1	x	$F=A \oplus B$	XOR
0	1	1	0	x	$F=A \wedge B$	AND
0	1	1	1	x	$F=\bar{A}$	NOT
1	0	0	0	x	$F=\text{Rotate A and B}$	Shift operation

Fig II shows Proposed 1-bit ALU with a Shifter

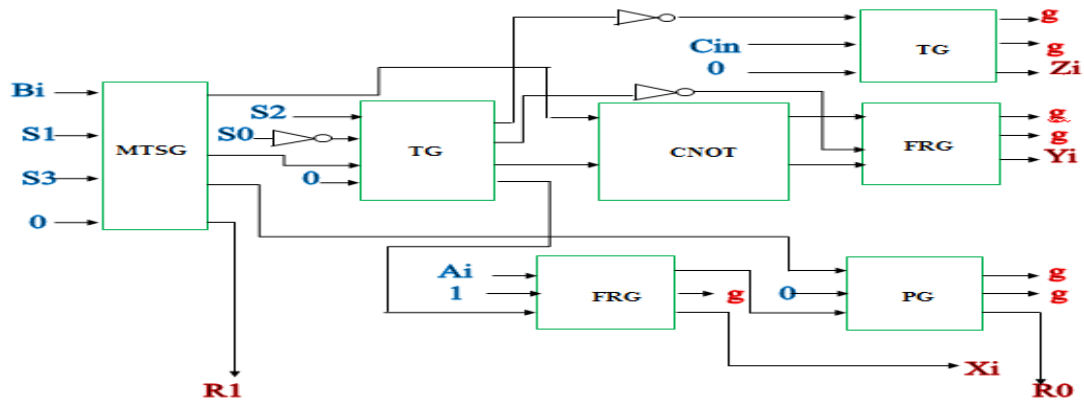
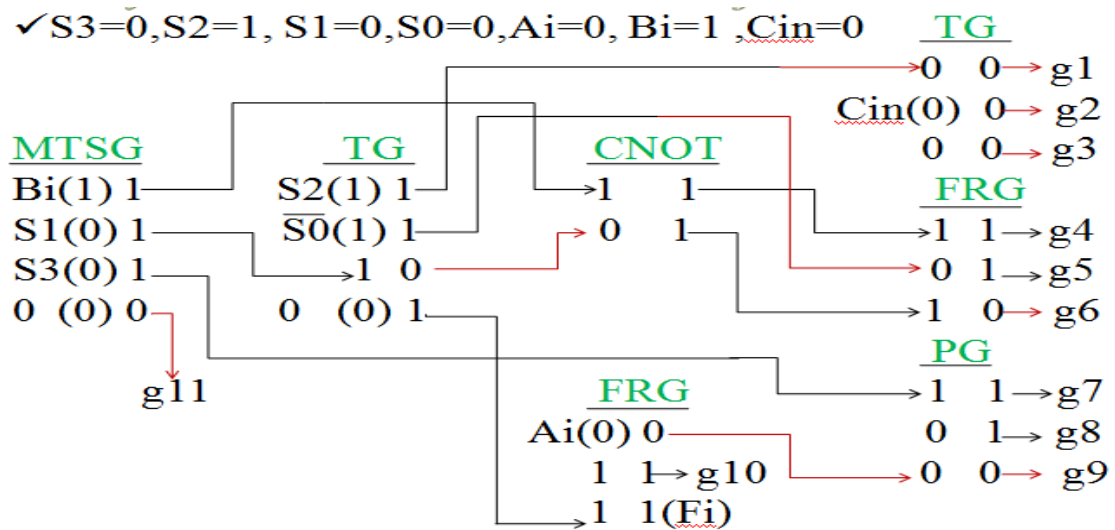


Fig III shows Synthesis of 1-bit ALU with a Shifter



V. Results & Disussion

The proposed Arithmetic Logic Unit can perform not only all arithmetic and logical operation with low power consumption but also shifting operation with the help of barrel shifter as well. The circuit has 4 constant input and 11 garbage output for Arithmetic-logic operations and 10 garbage output for shift operation. The proposed design implementation of Reversible arithmetic-Logic unit with Barrel shifter has better performance in terms of number of gates used, Garbage outputs and Quantum Cost and hence can be used for low power applications. In future, the design can be extended to any number of bits for Parallel Binary Adder/Subtractor unit and also for low power Reversible ALUs, Multipliers and Dividers.

VI. References

- [1] Landauer, R., 1961. Irreversibility and heat generation in The computing process", IBM J. Research and Development, 5(3) : 183-191.
- [2] Robert K Brayton, Sunil P Khatri "Multi-valued Logic Synthesis" University of California, Berkeley, CA 94720.
- [3] Himanshu Thapliyal and M.B Srinivas" A Beginning in the Reversible Logic Synthesis of Sequential Circuits" Centre for VLSI and Embedded System Technologies International Institute of Information Technology, Hyderabad, 500019, India.
- [4] Min-Lun Chuang, Chun-Yao Wang " Synthesis of Reversible Sequential Elements" Department of Computer Science, National Tsing Hua University, HsinChu, Taiwan R.O.C.

- [5] H.R.Bhagyalakshmi, M.K.Venkatesha” Optimized reversible BCD adder using new reversible logic gates” JOURNAL OF COMPUTING, VOLUME 2, ISSUE 2, FEBRUARY 2010, ISSN 2151-9617
- [6] Siva Kumar Sastry Hari Shyam Shroff Sk. Noor Mohammad V. Kamakoti” Efficient Building Blocks for Reversible Sequential Circuit Design” Department of Computer Science and Engineering, Indian Institute of Technology, Madras, Chennai - 600 036, India.
- [7] Alejandro Y. Pérez V.” Reversible Adder Implementation in VHDL” Digital Design Using HDL (ECE 590) Portland State University, Spring 2006.
- [8] H.R.Bhagyalakshmi, M.K.Venkatesha” Optimized reversible BCD adder using new reversible logic gates” JOURNAL OF COMPUTING, VOLUME 2, ISSUE 2, FEBRUARY 2010, ISSN 2151-9617.
- [9] Rangaraju H G, Venugopal U, Muralidhara K N, Raja K B” Low Power Reversible Parallel Binary Adder/Subtractor” Department of Telecommunication Engineering, Bangalore Institute of Technology, Bangalore, India.
- [10] Behrooz Parhami” Fault-Tolerant Reversible Circuits” Department of Electrical and Computer