



Design and Synthesis of Combinational Circuits Using Reversible Decoder

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Abstract—Reversible logic is one of the main emerging field for research in present era. The Reversible decoder is designed using Fredkin gates with very low minimum Quantum cost. There are many reversible logic gates like Fredkin Gate, Feynman Gate, TR gate, Double Feynman Gate, fredkin gate, Peres Gate, and many more. Reversible logic is referred as the total number of input lines are equal to the number of output lines i.e., there is a one to one mapping between the input and output vectors. The reversible gate must run forward and backward that means the inputs and outputs can be retrieved from both the sides. Reversible Logic has owns its many applications in various fields which include Quantum Computing, quantum-dot cellular automata (QCA), Optical Computing, Nanotechnology, Computer Graphics, low power VLSI Etc., Due to its low power consumption Reversible logic is gaining its own importance in recent years. The main aim of this paper is to realize different types of combinational circuits like decoder circuits, comparator, full adder/ subtractor, multiplexer, and encoder using reversible decoder circuit and the optimized reversible decoder is also proposed in this paper, it is highly optimized comparatively to all the existing designs. The analysis to be carried out in terms of garbage outputs, numbers of gates are also presented. The Circuit has been simulated and synthesized using Altera Quartus-II software.

Keywords: Quantum Cost, Reversible Gates, Garbage Outputs.

I. Introduction

Now a day, in VLSI Technology, the Power Consumption has become a highly important factor in electronic world. By using optimized Reversible Decoder for designing of Combinational, circuits power consumption is reduced to an optimum when compared to conventional decoder based combinational circuits. Reversible Logic has owns its many applications in various fields which include Quantum Computing[1], quantum-dot cellular automata (QCA), Optical Computing, Nanotechnology, Computer Graphics, low power VLSI. The main goal of the Low power VLSI is reduction of power dissipation [2, 6]. In the concept of conventional logics, while propagating the data from input to output, there is some part of information should be loss because of the power dissipation is highly intense, ultimately we are not properly getting reliable output to the input, all this process of bit data losses is proved by lauder. Finally, all these drawbacks should be overcome by the concept of reversible logic design. Ideally in reversible logics the power dissipation should be zero but in case of practical it has some minimum value. Internally there is a unique one-to-one mapping between the reversible logic gate[3,4] and the total number of inputs is equals to the number of outputs, this is the main reasons to reduce the information loss during the process of data propagation.

II. Definitions of Reversible Logic

1. **Garbage Output:** The unused outputs present in the outputs are referred as garbage.
2. **Number of reversible logic gates:** The number of reversible gates is used in the circuit.
3. **Delay:** it is the time taken by the circuit to propagation of inputs to the output.
4. **Ancillary bits:** The number of inputs which are maintained either constant 0 or 1 at the input.
5. **Quantum cost:** The number of 1X1 & 2X2 reversible logic gates or quantum logic used in the design.

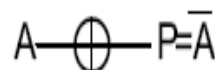
III. Existing Reversible Logic Gates

NOT GATE: It is a 1*1 gate reversible NOT Gate with zero Quantum Cost shown in figure 1.

Figure1 logic diagram



Figure2.1 Quantum implementation



Feynman Gate: It is also known as CNOT gate. It is a 2*2 reversible logic gate shown in fig 2.

Figure 2 Feynman gate

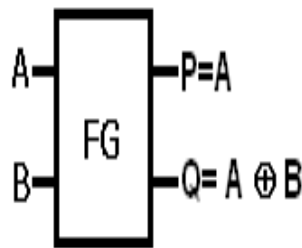
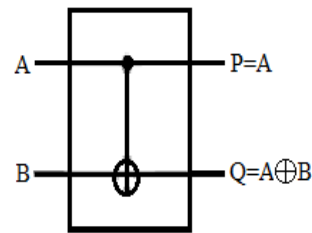


Figure 2.1 Quantum implementation



Double Feynman Gate: It is a 3*3 Feynman double logic gate with the quantum cost of 2 shown in fig 3.

Figure 3 Logic diagram

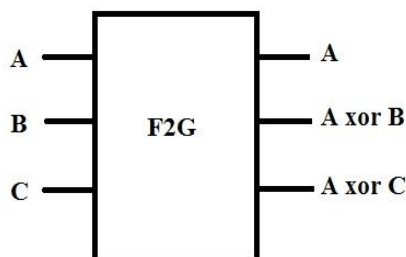
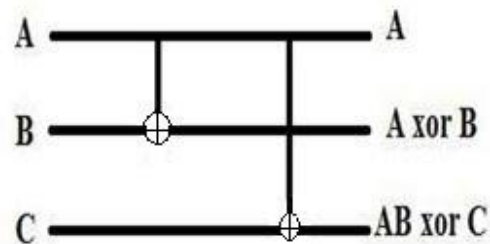


Figure 3.1. Quantum implementation



Peres Gate: It is a 3*3 Peres logic gate with the quantum cost of 4 shown in fig 4.

Figure 4 Logic gate

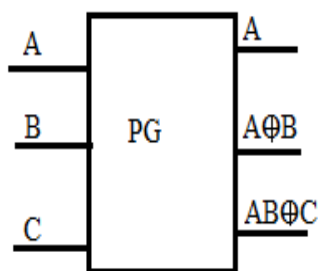
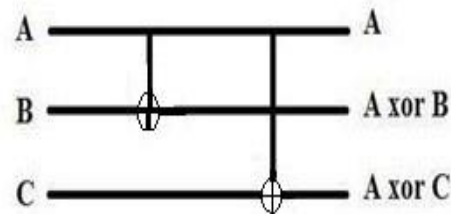


Figure 4.1 Quantum implementation



Toffoli Gate: It is a 3*3 toffoli logic gate with the quantum cost of 5 shown in fig 5. It called also CCNOT gate, invented by tommasotoffoli, is a universal reversible logic gate, which means that any reversible circuit can be constructed from Toffoli gates.

Figure 5 Logic gate

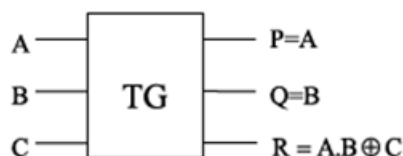
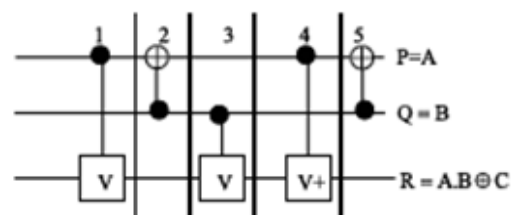


Figure 5.1 Quantum implementation

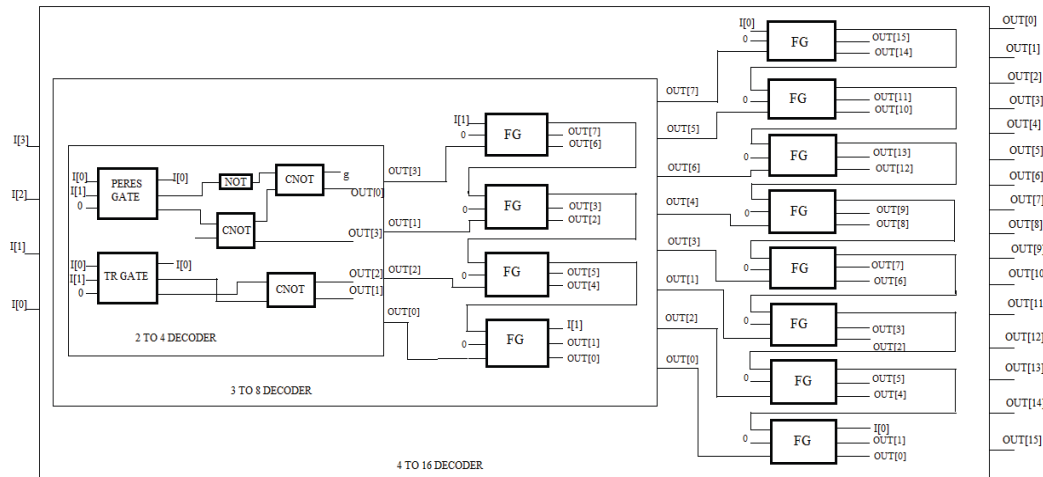


IV. Existing Method

The Combinational and Sequential Circuits are very important for designing of any digital circuits and it has been ongoing in research topic. Various proposals are given for the design of combinational circuits like adders, subtractors[5], comparators, multiplexers, decoder set., in the existing method the author

has given a novel design of 4x16 decoder whose Quantum Cost is less than the previous design [7]. Replacing Fredkin gates for designing 2x4 decoder reversible gates like Peres gate, TR gate, NOT gate and CNOT gate are used. The whole design is done using Fredkin gate, CNOT gate, Peres gates which give better Quantum Cost when compared to the other reversible Logic gates. The number of gates required to design 4x16 decoder are 18 in which there are 12 Fredkin gates [8], one Peres gate, one TR gate, one NOT gate and 3 CNOT gates. The sum of all the quantum costs of each gate gives total quantum cost of a 4x16 decoder.

Figure 6 Reversible decoders (2x4, 3x8 & 4x16)



V. Proposed Method

The Reversible existing 4x16 Decoder circuits are optimally designed than the existing designed by using this proposed decodes we can design the many more combinational circuit designs like 4 bit full adder/subtractor [9], 16*1 multiplexer, 1*16 decoder and the 16*4 encoder is also proposed which is not in the existing designs. All these proposed combinational designs are highly optimized interns of gate count, quantum cost and speed of the circuit [10].

Figure 7 Proposed reversible decoders (2x4 3x8 & 4x16).

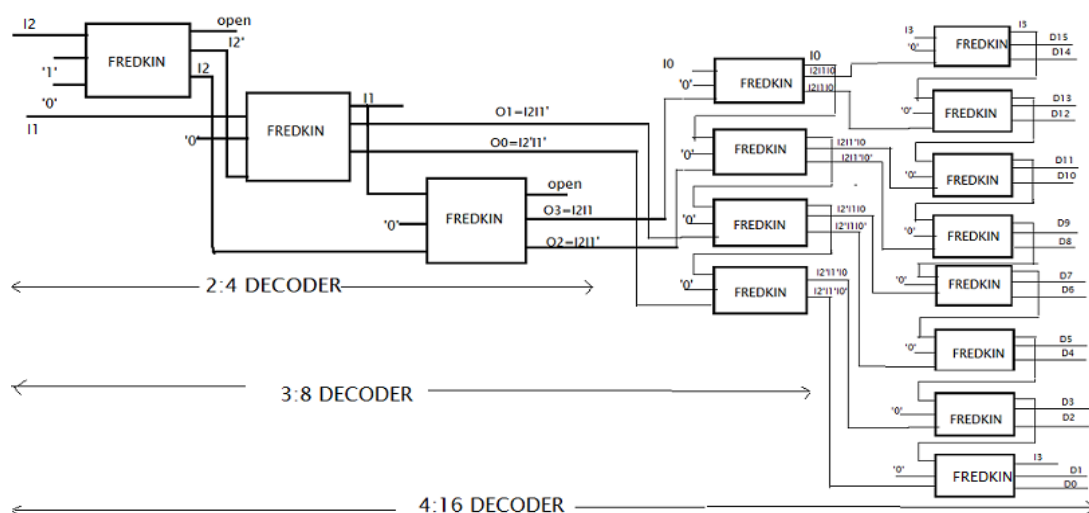


Figure 8 Reversible comparator

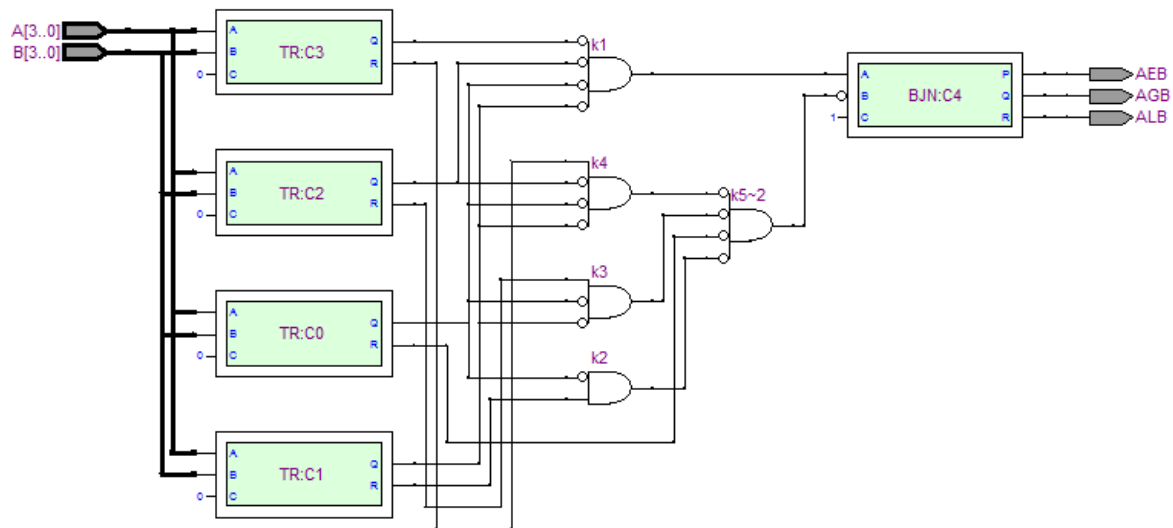


Figure 9 Full adder /subtractor

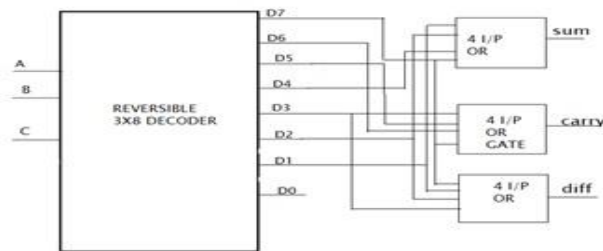
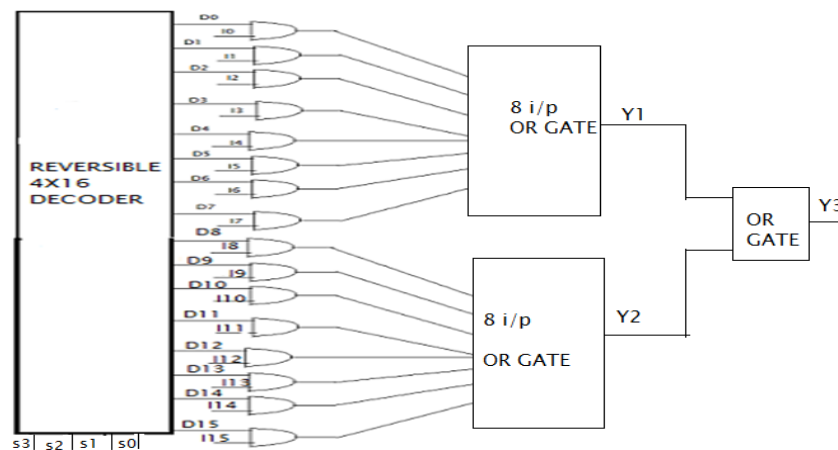


Figure 10 16x1 multiplexer using reversible 4x16 decoder



VI. Simulation Results

Figure 11 Simulation for 4:16 decoder

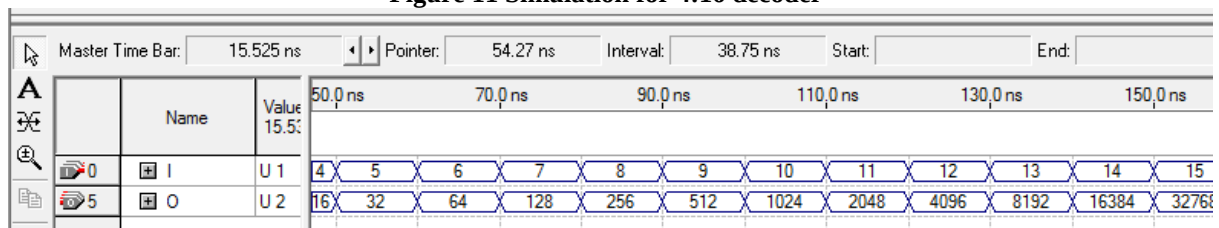


Figure 12 Simulation results for 4 bit comparator

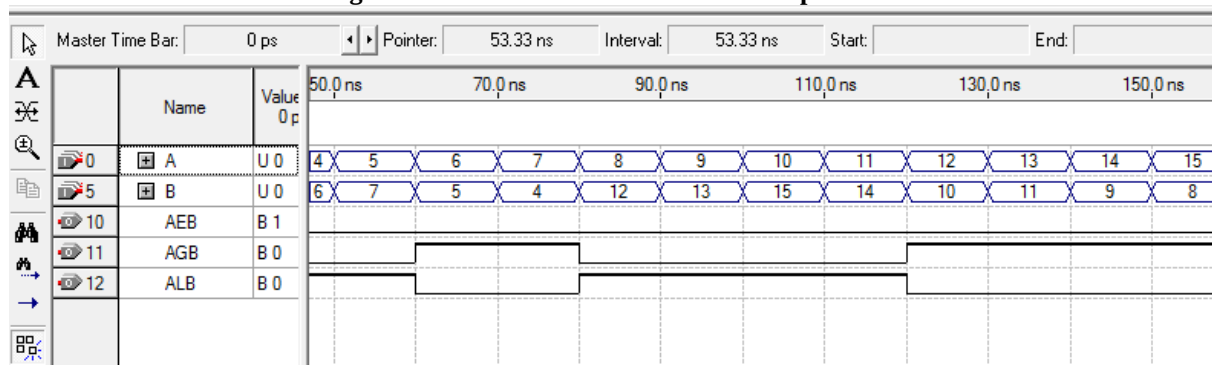


Figure 13 Simulation results for Full adder/subtractor

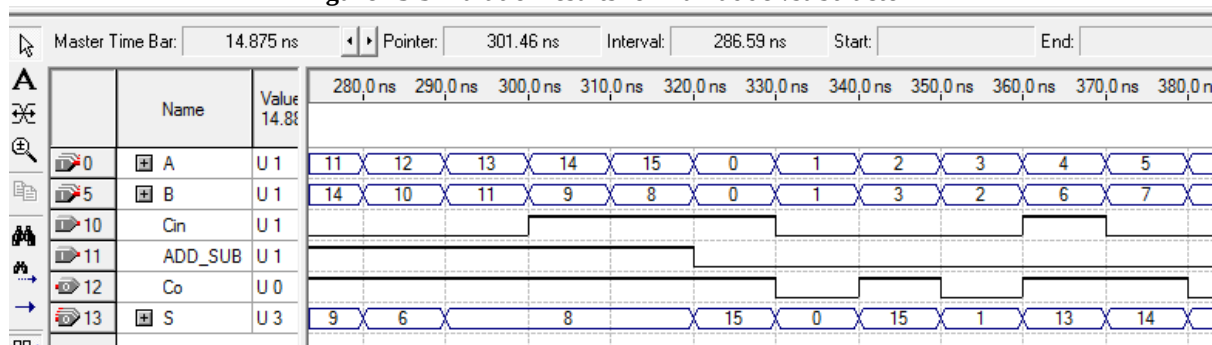


Figure 14 Simulation results for 16x1 Multiplexer

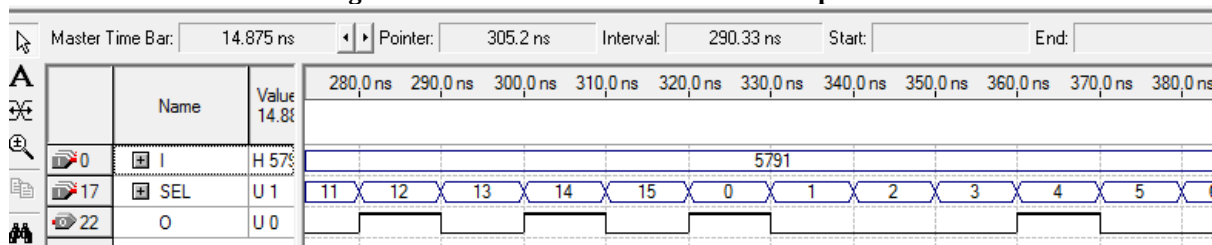
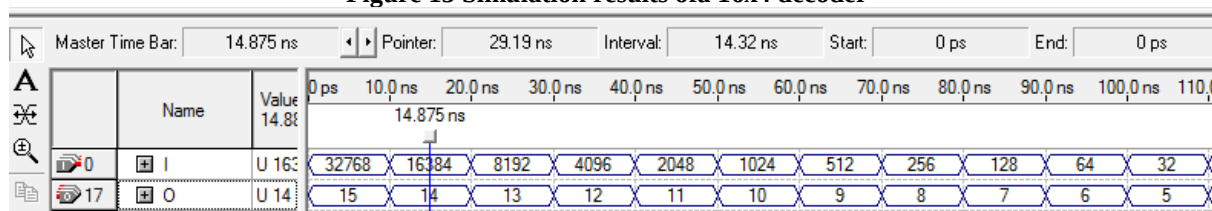


Figure 15 Simulation results of a 16x4 decoder



VII. Comparative Analysis

S.No	Proposed Reversible combinational logic circuit	Number of LUT's	Time Delay (ns)
1	4x16 Decoder	16	10.649
2	4 bit comparator	5	10.376
3	4 bit full adder/subtractor	9	10.559
4	16x1 multiplexer	8	9.918
5	16x4 encoder	40	10.969

VIII. Conclusion

In this paper, the combinational circuits are proposed like decoder circuits, comparator, full adder/subtractor, multiplexer, and encoder circuit's constructed using reversible decoder are designed. These circuits are designed for number of LUT's and Time Delay. The method proposed for designing the decoder circuit can be generalized. For example, a 3x8 decoder [11] can be designed using a 2x4 decoder followed

by 4 Fredkin gates, similarly a 4×16 decoder can be designed using 3×8 decoder followed by 8 Fredkin gates. The concept of duplicating the single output required number of outputs is utilized to overcome the fan-out limitation in reversible logic circuits. This method of designing combinational circuits helps to implement many digital circuits with better performance in terms of time delay. All these proposed combinational circuits are highly optimized in terms of number of LUT's and Time Delay.

IX. References

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