



Lyapunov Stability Analysis of Three Phase Three Wire DSTATCOM

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Abstract: This paper presents the Lyapunov stability analysis of three-leg Voltage Source Inverter (VSI) as a Distribution Static Compensator (DSTATCOM) topology for a three phase three wire system with unbalanced and nonlinear loads. The VSI based DSTATCOM topology for the given system is operated in current controlled mode using appropriate strategy such that the compensator currents are injected to achieve harmonics mitigation, power factor correction and reactive power compensation. The tracking of reference currents obtained is done using Synchronous Reference Frame (SRF) method. The conditions necessary for stabilized and controllable switching is obtained by Lyapunov stability criteria. Simulation studies have been performed in MATLAB. The DSTATCOM topology and is found to be effective in reducing supply harmonics, load demand balancing and power factor correction. SIMULINK results have been generated in order to verify the various claims.

Keywords: Voltage Source Inverter, VSI, Distribution Static Compensator, DSTATCOM, three phase three wire system, stability.

I. Introduction

Inverters are now used in a wide variety of applications such as Static VAR Sources (SVCs), Static Synchronous Compensators (STATCOM) [1], Active Power Filters [2], Adjustable Speed Drives (ASDs) for medium voltage Induction Motors, Active Power Filters [2], etc. One of the applications of inverters finds its use in Distribution Static Compensator (DSTATCOM).

DSTATCOM consists of a VSI with DC storage capacitor connected across leg of VSI, which is connected at distribution side of given three phase system. The VSI is operated by current controlled mode by use of appropriate strategy [3]. The DSTATCOM topologies are available for both three phase three wire systems and three phase four wire systems [4].

The three phase three wire DSTATCOM topologies are classified into two categories namely (i) isolated VSI based DSTATCOM topology and (ii) Non-isolated VSI based DSTATCOM topology. These topology are further classified as (i): (a) Three leg VSI, (b) Two leg VSI with split capacitor; (ii) (a) Three single phase VSI (b) Three leg VSI using star-delta transformer (c) Two leg VSI using star-delta transformer. The three phase four wire DSTATCOM topology has been explained in literature [5].

This paper represents three leg VSI based topology of DSTATCOM for given three phase three wire system which can compensate unbalanced load as well as nonlinear load. The topology consists of a three leg VSI with a single capacitor connected across its leg.

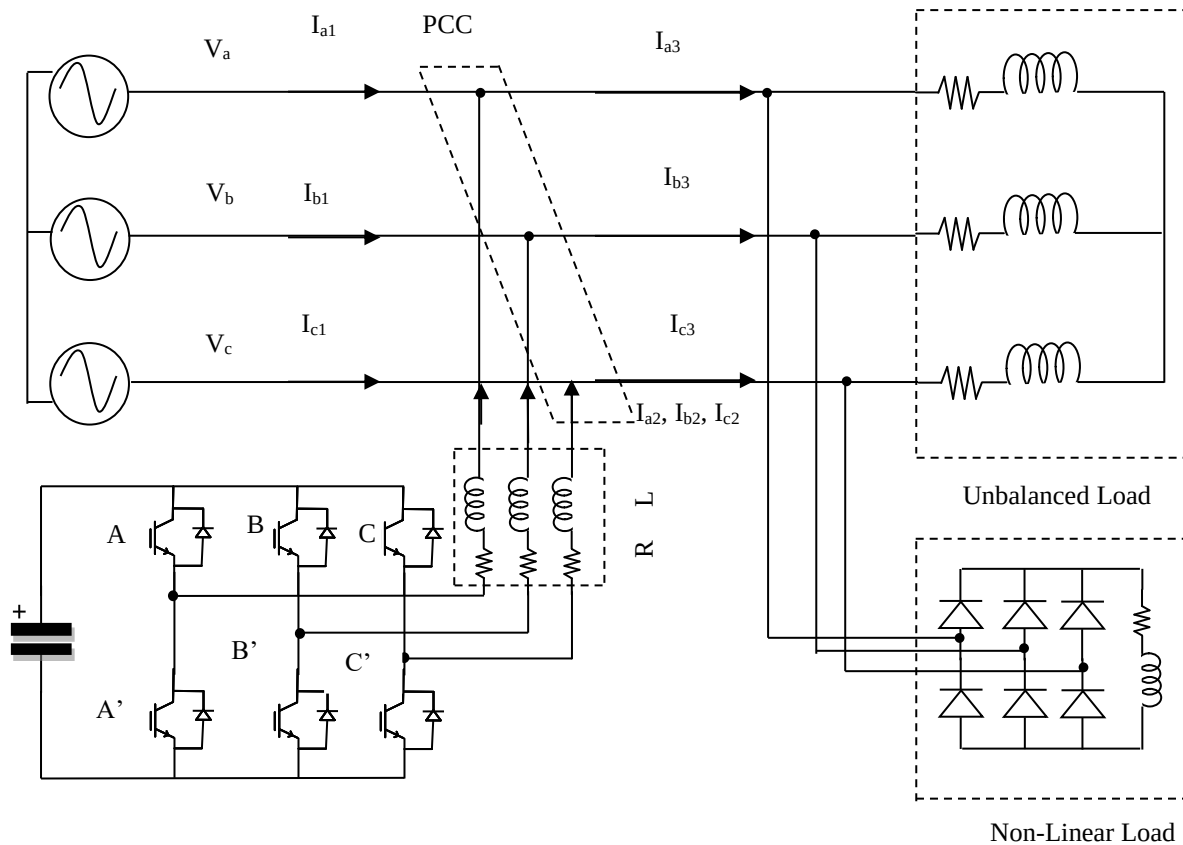
The VSI operates in a total number of (2^3) eight states, starting from state '000' to state '111', out of which state '000' and state '111' are uncontrollable and are termed as zero vector state. Therefore, VSI is made to operate from state '001' to state '110'.

Each of these states represents the switching of upper switches in the three legs named A, B and C respectively whereas the complement of given states is used for switching of lower switches of the three legs named A', B' and C' respectively. The considered DSTATCOM topology and its dynamic analysis have been explained in next section. The control of switching parameters of VSI in DSTATCOM has been done on the basis of Lyapunov stability Criteria.

II. Proposed Topology

Figure 1 represents the circuit of considered DSTATCOM topology used. The source voltages and currents for the three phases are given by V_a , V_b , V_c and I_{a1} , I_{b1} , I_{c1} respectively. The filter currents output from VSI corresponding to the three phases are given by I_{a2} , I_{b2} and I_{c2} respectively whereas the load current for the three phases are given by I_{a3} , I_{b3} and I_{c3} respectively.

Figure 1: DSTATCOM Topology



The interfacing filter parameters are represented by resistance R and inductance L for each phase respectively. The load parameters are represented by resistance R_L and inductance L_L respectively. The non-linear load consists of diode rectifier with given single phase RL load. The DC link capacitor is represented by C_{DC} and voltage stored by the corresponding capacitor is given by V_{DC} .

The equation for phase A operation is as follows:

$$2L_a \frac{di_{a2}}{dt} - L_b \frac{di_{b2}}{dt} - L_c \frac{di_{c2}}{dt} = (A \cdot x - \bar{A} \cdot y)V_{DC} - 2V_a + V_b + V_c - 2RI_{a2} + R_b I_{b2} + R_c I_{c2} \quad (1)$$

Where, $x = (\bar{A} + \bar{B} + \bar{C})$, $y = (A + B + C)$ and A, B, C, A', B' and C' are switching functions corresponding to phase A, B and C.

Similarly, the equations used for describing switching operation of other two legs corresponding to phases B and phase C are as follows:

$$-L_a \frac{di_{a2}}{dt} + 2L_b \frac{di_{b2}}{dt} - L_c \frac{di_{c2}}{dt} = (B \cdot x - \bar{B} \cdot y)V_{DC} + V_a - 2V_b + V_c + RI_{a2} - 2R_b I_{b2} + R_c I_{c2} \quad (2)$$

$$-L_a \frac{di_{a2}}{dt} - 2L_b \frac{di_{b2}}{dt} + L_c \frac{di_{c2}}{dt} = (C \cdot x - \bar{C} \cdot y)V_{DC} + V_a + V_b - 2V_c + RI_{a2} + R_b I_{b2} - 2R_c I_{c2} \quad (3)$$

The equation showing voltage dynamics of DC storage capacitor C_{DC} is as follows:

$$C_{DC} \frac{dV_{DC}}{dt} = (\bar{A} - A)I_{a2} + (\bar{B} - B)I_{b2} + (\bar{C} - C)I_{c2} \quad (4)$$

The state model for the system, given I_{a2}, I_{b2}, I_{c2} and V_{DC} are the states, is given by the equation below:

$$M \cdot \dot{x} = A \cdot x + B \cdot u \quad (5)$$

The matrices for the state model represented by equation (5) are as follows:

$$x = \begin{bmatrix} I_{a2} \\ I_{b2} \\ I_{c2} \\ 2V_{DC} \end{bmatrix} \quad A = \begin{bmatrix} -2R_a & R_b & R_c & A \cdot x - A' \cdot y \\ R_a & -2R_b & R_c & B \cdot x - B' \cdot y \\ R_a & R_b & -2R_c & C \cdot x - C' \cdot y \\ A' - A & B' - B & C' - C & 0 \end{bmatrix} \quad (6)$$

$$M = \begin{bmatrix} 2L_a & -L_b & -L_c & 0 \\ -L_a & 2L_b & -L_c & 0 \\ -L_a & -L_b & 2L_c & 0 \\ 0 & 0 & 0 & C_{d.c.} \end{bmatrix} u = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad B = \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \\ 0 & 0 & 0 \end{bmatrix} \quad (7)$$

For given state model, matrix M is constant. In order to obtain the solution of the given state model, the state model is converted to the form $\dot{x} = M^{-1}.A.x + M^{-1}.B.u$. However, M^{-1} does not exist for the given model because matrix M does not possess full rank 4. This is because of the dependence of one of the given states on other states as given by the following equation:

$$I_{a2} + I_{b2} + I_{c2} = 0 \quad (8)$$

Reducing the order of state model to by substituting I_{c2} , equation (5) is converted to the equation below:

$$m.\dot{x} = a.x + b.u \quad (9)$$

$$x = \begin{bmatrix} I_{a2} \\ I_{b2} \\ V_{DC} \end{bmatrix} \quad a = \begin{bmatrix} -2R_a - R_c & R_b - R_c & A.x - \bar{A}.y \\ R_a - R_c & -2R_b - R_c & B.x - \bar{B}.y \\ (\bar{A} - A) - (\bar{C} - C) & (\bar{B} - B) - (\bar{C} - C) & 0 \end{bmatrix} \quad (10)$$

$$m = \begin{bmatrix} 2L_a + L_c & -L_b + L_c & 0 \\ -L_a + L_c & 2L_b + L_c & 0 \\ 0 & 0 & C_{d.c.} \end{bmatrix} u = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} b = \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 0 & 0 & 0 \end{bmatrix} \quad (11)$$

Matrix m is now invertible and state equation can now be solved.

III. Lyapunov Stability Criteria for Switching Control

For solution of tracking current, the state I_{a2} , I_{b2} and I_{c2} are needed to follow the extracted reference currents obtained by use of load compensation algorithm such as instantaneous symmetrical component theory or p-q theory. For the balanced set of voltages, the dynamics of the inductor currents are being considered and filter resistance and inductance in all phases are assumed such that:

$$\frac{dI_2}{dt} = \frac{(Z.x - \bar{Z}.y)2V_{DC}}{3L} - \frac{RI_2}{L} - \frac{V}{L} \quad (12)$$

Where, V is source voltage and I_2 is corresponding filter current for any of three phases. For determination of DC link voltage, the following positive definite lyapunov function such that its derivative with respect to time is needed to be negative definite.

$$V = \frac{1}{2}(w_p - w_{refp})^2; p = a, b, c \quad (13)$$

Where, w_p and w_{refp} are actual and reference state of any of the phases. The derivative of Lyapunov equation is obtained as follows:

$$\dot{V} = (\dot{w} - \dot{w}_{ref})(w - w_{ref}) \quad (14)$$

Due to difference in slope of actual and reference currents, the value of time derivative of Lyapunov function V is approximated to the following equation below:

$$\dot{V} = (\dot{w})(w - w_{ref}) \quad (15)$$

Substituting actual state by I_2 and using equation (15), we get:

$$\dot{V} = \left\{ -\frac{R}{L}I_2 - \frac{V}{L} + \frac{(Z.x - \bar{Z}.y)2V_{DC}}{3L} \right\} (I_2 - \bar{I}_2) \quad (16)$$

Where, Z and $\bar{Z}$ are switching states of the upper and lower switches in any of the phase and x and y are as defined in equation (1). Considering the error is positive, the control is such that $Z=0$ and $\bar{Z}=1$. Hence, the derivative of Lyapunov equation becomes negative only when the following equation below is found to be true.

$$\frac{V_{DC}}{3}y > -RI_2 - V \quad (17)$$

If the error is considered to be negative, the derivative of Lyapunov equation becomes negative only when the equation below is found to be true.

$$\frac{V_{DC}}{3}x < RI_2 + V \quad (18)$$

To ensure negative definiteness of equation (16), conditions provided by equation (17) and (18) have been satisfied. It has also been obtained from the results that the voltage applied for particular state should sufficiently overcome resistive drop and source voltage for effective current tracking.

IV. Simulation Studies

Table 1: Simulation Parameters

SUPPLY VOLTAGE	415 V,50Hz
DC CAPACITOR(C_{DC})	2500 μ F
DC LINK VOLTAGE (V_{DC})	750 V
INTERFACING INDUCTOR(L,R)	3.5mH,1 Ω
UNBALANCED LOAD	Phase a :25 Ω ,0.5mH Phase b :44 Ω ,8.11mH Phase c :50 Ω ,2.75mH
NONLINEAR LOAD	Diode rectifier with constant RL load of 10 Ω , 10mH

Table 1 shows the various simulation parameters used in the considered DSTATCOM topology. Based on the mathematical model derived, simulation was done on a three phase three wire system. The compensator consists of three-leg voltage source inverter having six switches with an anti-parallel diode connected across each switch. The VSI is connected to three phase three wire system at PCC by use of an interface filter which consists of and inductor L whose resistance is R. DC link voltage is regulated to V_{DCref} with help of PI controller. The supply voltages from the grid are considered to be balanced and sinusoidal. Figure 2 (a), (b) and (c) shows source voltages, source currents, and load voltages for the phases a, b and c respectively. Figure 2 (d) shows the load current waveforms for nonlinear loads. The reference current obtained are tracked by SRF method. Figure 3 shows VSI parameters such as DC link voltage across capacitor C_{DC} , compensator/VSI voltages and currents for phase a, b and c respectively.

Figure 2: (a) Source Voltage (b) Source Current (c) Load Voltage (d) Load Current.

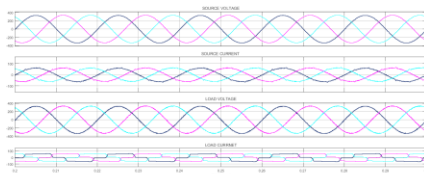
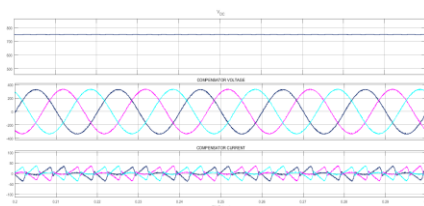


Figure 3: (a) DC Link Voltage (b) Compensator Output Voltage (c) compensator output current.



V. Conclusion

The model for given three leg VSI based DSTATCOM topology has been designed. Lyapunov stability criterion was used for selection of value of DC link voltage that is to be used to ensure controllable and stable switching. Simulations have been performed and the compensating system was found to be effective in harmonics mitigations, power factor correction and reactive power compensation for three phase three wire system with nonlinear loads with which the effectiveness of the given DSTATCOM topology has been confirmed.

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