



## Design of CMOS Ring VCO for PLL based Frequency Synthesizer using different aspect ratios of MOS transistors

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**Abstract:** The voltage controlled oscillator is one of the most important building blocks of the PLL based frequency synthesizer. This paper presents the design of CMOS Ring VCO for PLL based Frequency Synthesizer using different aspect ratios of MOS transistors. A three stage ring VCO is designed in 180nm CMOS technology under the supply voltage of 1.8V and achieves a high oscillation frequency of 5.2GHz. With an increase in the aspect ratio of the MOS transistors, the frequency of oscillation becomes 5.5GHz.

**Keywords:** Ring Oscillator, VCO, PLL, Inverter, Time Delay, Oscillation Frequency, Aspect Ratio.

### I. Introduction

A frequency synthesizer is a circuit design that generates a new frequency from a single stable reference frequency. A crystal oscillator is often used for the reference frequency. The main objective of frequency synthesizer is to recover the signal without phase and frequency error and this process is completed after many iterations inside the system. The fundamental functional blocks of any frequency synthesizer in general are

- i) Phase frequency detector (PFD)
- ii) Charge Pump (CP)
- iii) Low pass filter (LPF)
- iv) Voltage Controlled Oscillator (VCO)
- v) Loop Divider

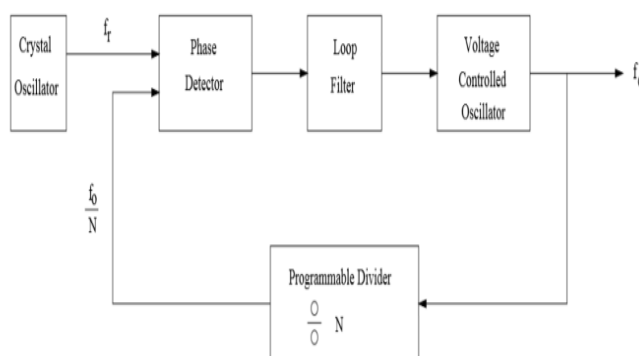


Fig. 1: Frequency Synthesizer Block Diagram

Today's trend in the design of frequency synthesizer is the use of PLL as the underlying technology leading to coherent Indirect Synthesis. Prior to this, direct frequency synthesis concept was there in which the output frequency is generated by adding signals from many oscillators through a combination of frequency mixing and remixing [1]. Moreover, the technology that has been used in direct synthesis is that of BJT and the frequency is obtained in the range of 5 kHz to 100 MHz. Channel spacing that has been used is in the range of 5kHz to 10 KHz. The direct frequency synthesizer has no feedback loop and no VCO.

The trend of today is the design of indirect frequency synthesizer comprising of PLL (phase detector, charge pump, VCO) and loop divider circuit. Researchers have designed VCO for frequency synthesizers using CMOS technologies starting from 1 $\mu$ m upto 90nm. The frequencies that have been achieved is in the range of 10MHz to 6

GHz [4][6][8][9][10]. In this proposed work, CMOS based VCO for indirect frequency synthesizer has been designed using different aspect ratios of the MOS transistors.

## II Ring VCO CMOS Topology

In the proposed work a three stage Ring VCO for PLL based Frequency Synthesizer with different aspect ratio of MOS transistor has been designed. Ring VCO which consists of inverters is shown in fig 2. For oscillation occurrence, the ring must provide a phase shift of  $2\pi$  and should have unity voltage gain. Each delay stage should provide a phase shift of  $\pi/N$  where  $N$  is number of delay stages. The remaining  $\pi$  phase shift is provided by dc inversion. Single ended oscillator requires odd number of stages for dc inversion.

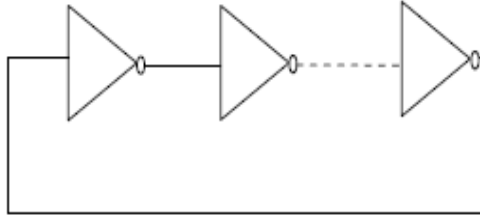


Fig 2. Block diagram of single ended Ring VCO [4]

Assuming the inverters are identical, the oscillation frequency is given as follow

$$f_{osc} = 1 / (2 * n * (t_{phl} + t_{plh})) \quad (1)$$

where  $n$  is the number of inverters in the ring oscillator and  $(t_{phl} + t_{plh})$  is the propagation delay of each inverter. The propagation delay times  $t_{phl}$  and  $t_{plh}$  determine the input-to-output signal delay during to high-to-low and low-to-high transitions of output respectively [5].

$$t_{phl} = (C_{load} / k_n (V_{dd} - V_{tn})) * [(2 * V_{tn}) / (V_{dd} - V_{tn}) + \ln((4(V_{dd} - V_{tn}) / V_{dd}) - 1)] \quad (2)$$

$$t_{plh} = (C_{load} / k_p (V_{dd} - V_{tp})) * [(2 * V_{tp}) / (V_{dd} - V_{tp}) + \ln((4(V_{dd} - V_{tp}) / V_{dd}) - 1)] \quad (3)$$

The first stage CMOS inverter of ring VCO with the single lumped output load capacitance is shown in figure 3. When the input voltage switches from low to high, the PMOS transistor in the circuit is turned off and the NMOS transistor starts conducting. During this phase, the output load capacitance is being discharged through the NMOS transistor. Thus the capacitor current equals the instantaneous drain current of the NMOS transistor. When the input voltage switches from high to low, the NMOS transistor in the circuit is turned off and the PMOS transistor starts conducting. During this phase, the output load capacitance is being charged up through the PMOS transistor therefore the capacitor current equals the instantaneous drain current of the PMOS transistor [5]. The drain current is proportional to the ratio of the channel width to the channel length.

$$I_D = (\mu_n C_{ox} / L) * (W/L)_1 * (V_{th} - V_{tn})^2 \quad (4)$$

The logic threshold voltage of the CMOS inverter is given as [5]

$$V_{th} = V_{To,n} + (1/k_R)^{1/2} (V_{dd} + V_{To,p}) / (1 + (1/k_R)^{1/2}) \quad (5)$$

Where ratio  $k_R$  is given by

$$k_R = (\mu_n C_{ox} (W_n / L_n)) / (\mu_p C_{ox} (W_p / L_p)) \quad (6)$$

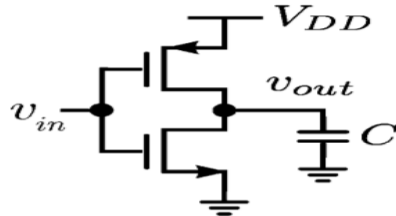


Fig 3: CMOS inverter driving a capacitor load as in a Ring VCO [11]

The output load capacitance is given as follows [5].

$$C_L = C_{gdn} + C_{gdp} + C_{dbn} + C_{dbp} + C_{int} + C_g \quad (7)$$

where  $C_L$  is the Load Capacitance

$C_{db}$  is the drain substrate junction capacitance and is given by

$$C_{db} = A * C_{j0} * K_{eq} + P * C_{jsw} * K_{eq(sw)} \quad (8)$$

where  $C_{j0}$  is the zero bias junction capacitance per unit area.  $C_{jsw}$  is the zero bias side wall junction capacitance per unit length.  $K_{eq}$  is the voltage equivalence factor ( $0 < K_{eq} < 1$ ) [5].

$$C_{jsw} = C_{j0sw} * X_j \quad (9)$$

$$C_{j0} = (\epsilon_{si} * q / 2 * ((N_A * N_D) / (N_A + N_D)) * 1 / \phi_0)^{1/2} \quad (10)$$

$$C_{j0sw} = \epsilon_{si} * q / 2 * ((N_{A(sw)} * N_D) / (N_{A(sw)} + N_D)) * 1 / \phi_{0sw})^{1/2} \quad (11)$$

where

$N_A$  = Substrate Doping and  $N_D$  = Source/ Drain Doping and  $A$  is the junction bottom area and  $P$  is the junction sidewall parameter [3].

$C_{gd}$  is gate to drain capacitance. It is actually the gate to channel capacitance seen between the gate and the drain terminals [3].

$$C_{gd} = C_{ox} * W * L_D \quad (12)$$

Where  $L_D$  is the lateral diffusion of the source or drain under the gate. The value of  $L_D$  is taken as .05 $\mu$ m.

The gate oxide capacitance is defined by [3]

$$C_g = W * L * C_{ox} \quad (13)$$

The gate oxide capacitance per unit area is given by

$$C_{ox} = \epsilon_{ox} / t_{ox} \quad \dots\dots\dots (14)$$

where  $\epsilon_{ox} = 3.45 * 10^{-11}$  F/m and is called the permittivity of the silicon oxide.

$t_{ox}$  is called the oxide thickness. The oxide thickness is determined by the process technology used to fabricate the MOSFET. The value of  $t_{ox}$  is 4nm in 180 nm technology.

Usually the channel lengths  $L_n$  and  $L_p$  are usually fixed and equal to each other. The transistor aspect ratio [5] is defined as

$$R(\text{aspectratio}) = W_p / W_n \quad (15)$$

### III. Results and Discussion

The performance comparison of three stage Ring VCO in terms of oscillation frequency for different values of W/L ratios of MOS transistors in 180nm technology is given below:

- When  $(W/L)_n = 0.36/0.18$  and  $(W/L)_p = 1.08/0.18$  then the Oscillation Frequency is 5.2GHz.
- When  $(W/L)_n = 0.36/0.18$  and  $(W/L)_p = 1.44/0.18$  then the Oscillation Frequency is 5.5GHz.
- When  $(W/L)_n = 0.54/0.18$  and  $(W/L)_p = 1.62/0.18$  then the Oscillation Frequency is 6.2GHz.

### IV. Conclusion

In this paper the design of three stage ring VCO for PLL based frequency synthesizer with different aspect ratio of MOS transistor has been proposed. It is observed that increasing aspect ratio of MOS transistor decreases  $\tau_{ph}$  because of increased current available to charge load capacitance as drain current is proportional to the ratio of channel width  $W$  to the channel length  $L$ .

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