



Design of PLL Based Frequency Synthesizer Using Charge Pump

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Abstract: This paper presents a design of PLL based Frequency Synthesizer. The various functional blocks of frequency synthesizer are explained. In this paper we describe the effect of loop filter resistance on lock time and obtain minimum lock time for a particular value of loop filter resistance. The charge pump current is evaluated for different values of phase difference between the two pulses at the phase frequency detector and the corresponding control voltage generated at input of the VCO is also evaluated. It has been observed that as the phase difference is increased, the error voltage and thus the charge pump current also increases. This result in an increase in the VCO control voltage. A two modulus loop divider design is also presented.

Keywords: Frequency Synthesizer, Phase frequency Detector, Charge Pump, VCO, Loop Divider, Loop Filter, Control Voltage.

I. Introduction

A frequency synthesizer is a circuit design that generates a new frequency from a single stable reference frequency. A crystal oscillator is often used for the reference frequency. The main objective of frequency synthesizer is to recover the signal without phase and frequency error and this process is completed after many iterations inside the system. The fundamental functional blocks of any frequency synthesizer are shown in fig. 1.

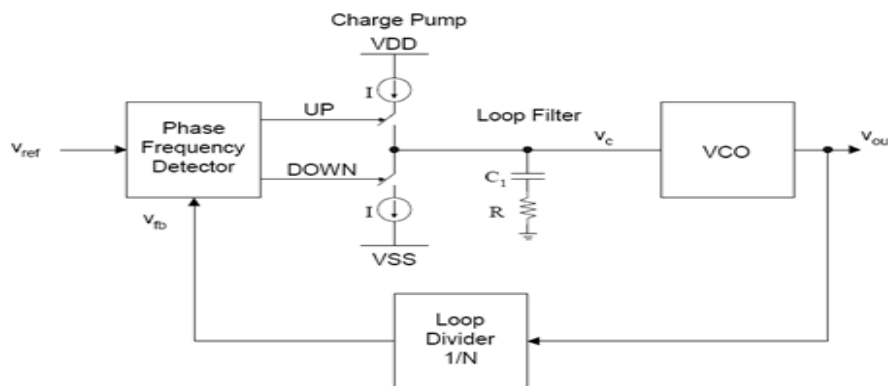


Fig. 1: Frequency Synthesizer – Functional Blocks

II. Frequency Synthesizer Architecture

The description of various blocks of Frequency Synthesizer are as follows:

A Phase Frequency Detector

The phase frequency detector compares the phase of an incoming reference signal with that of the VCO and produces some output that is some function of the phase difference.

B. The Charge Pump

A charge pump is a three position electronic device switch which is controlled by the three states of a PFD. When switch is set in UP or DOWN position, it delivers a pump voltage $\pm V_P$ or a pump current $\pm I_P$ to the loop filter. When both UP and DOWN of PFD are off, the switch is open thus isolating the loop filter from the charge pump and PFD. As shown in the fig 4 current sources I_{up} and I_{dn} are identical. Two outputs of PFD are given to the UP and DOWN inputs of charge pump respectively [2].

C. Loop Filter

The output of PFD consists of dc component superimposed with an ac component. The ac part

is undesired as an input to VCO. Hence low pass filter is used to filter out ac component. Both passive filter and active filter can be used but a passive filter is usually preferred than an active filter because an active filter results in higher complexity, cost and noise

D. VCO

A VCO is a voltage controlled oscillator whose output frequency is linearly proportional to the control voltage generated by the PFD and Loop Filter.

E. Loop Divider

The PLL reference clock is generated from a crystal. The crystal typically operates from tens to a few hundreds of MHz's. On the other hand VCO's operate at a high frequency. For proper functioning of the phase frequency detector, a frequency divider is necessary which divides down the VCO frequency to the frequency of the reference clock.

III. Proposed Work

A. Evaluation Of Lock Time

Phase locked loop is designed and lock time has been evaluated in this step.

Assume the time differences between the rising edges of the two pulses, the output current is evaluated corresponding to time difference [8]. The phase difference is given by

$$I_{PDI} = K_{PDI} \times \Delta\phi \quad (1)$$

$$\text{where } K_{PDI} = I_{PUMP} / 2\pi \text{ (amp/rad)} \quad (2)$$

Determine Damping Factor, ζ

The damping factor is set to yield an optimally flat frequency response. This results in ζ being equal to 0.707

Determine average VCO gain [8] as follows

$$K_{VCO} = 2\pi \cdot (f_{max} - f_{min}) / V \text{ (rad/sec)} \quad (3)$$

Determine Charge Pump Current and loop filter capacitor in the next step. The charge pump current is set so that a decent loop gain is obtained. Determine Natural Frequency as follows

$$\omega_{3db} = \omega_n \sqrt{(2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1})} \quad (4)$$

$$\omega_{3db} = \omega_n (2.06) \text{ at } \zeta = 0.7 \quad (5)$$

For system stability purpose, the Loop B.W. is taken to be at least or equal to 1/10 of the Reference Frequency. However, it is desirable to make the loop B.W. as wide as possible in order to suppress the VCO phase noise. In order to compromise between stability and noise performance, the loop B.W. is set to

$$\omega_{3db} = (\omega_{ref}/10) * 0.75 \quad (6)$$

Determine other loop filter components.

$$R = (2 * \zeta) / \omega_n * C \quad (7)$$

Thus the lock time has been evaluated using the following equations.

$$\text{Lock Time} = 2\pi / \omega_n \quad (8)$$

VCO gain is given [8] by

$$K_{VCO} = 2\pi \cdot (f_{max} - f_{min}) / V \text{ (rad/sec)}$$

Therefore $K_{VCO} = 10.46 \text{ MHz/V}$ (at $f_{max} - f_{min} = 930 - 927 \text{ MHz}$ and $V = 1.8$)

Assume Charge Pump Current = 32 μamp .

Assume the time differences between the rising edges of the two pulses be $\pi/2$

$$I_{PDI} = K_{PDI} \times \Delta\phi$$

$$\Delta\phi = (\Delta t / T_{clk}) * 2\pi$$

$$\text{where } K_{PDI} = I_{PUMP} / 2\pi \text{ (amp/rad)}$$

$$\text{Therefore } K_{PDI} = 32 / 2\pi \text{ (amp/rad) and}$$

$$I_{PDI} = (32 / 2\pi) * (1.25 / 5) * (2\pi) = 8 \mu\text{amp}$$

Assume the value of zeta as 0.7

$$\text{At } C_1 = 22 \text{ pF, } \omega_n = (2 * \zeta) / (R * C)$$

By varying the value of R and ζ keeping other quantities constant, the effect on Lock Time can be evaluated.

B. Evaluation Of Control Voltage

The Control Voltage can be obtained [5] as $V_{invco} = K_f * I_{pdi}$ (9)

$$K_f = 0.16 * 10^3$$

$$V_{invco} = 1.28 \text{ mV at phase diff of } \pi/2$$

C. Design of Loop Divider Circuit

The designed frequency synthesizer uses a two modulus divider. It consists of pre-scaler, a main counter, a swallow counter and a control unit.

i) Algorithm for Two Modulus Loop Divider

1. Load the Pre-Scalar with the Initial Value (P+1), (from Load Register).
2. Load the Swallow Counter A and the Main Counter M with Initial Values (from Load Registers). Value of M should be kept higher than A.
3. Each rising edge of clock pulse (from VCO) decrements the Pre-Scalar contents by 1.

4. If Pre-Scalar contents equal zero, decrement the Swallow and Main Counter contents each by 1 i.e. $A.Contents = A.Contents - 1$ and $M.Contents = M.Contents - 1$.
5. If $((A.Contents > 0) \text{ and } (M.Contents > 0))$, load Pre-Scalar with $(P+1)$ and go to Step 3.
6. If $((A.Contents = 0) \text{ and } (M.Contents > 0))$, load Pre-Scalar with P and go to Step 3.
7. If $((A.Contents = 0) \text{ and } (M.Contents = 0))$, load Pre-Scalar with $(P+1)$ and go to Step 2.
8. Go to Step 1 and repeat the process.
9. End

ii) Algorithm for Evaluating and Fixing the Values of P, M and A in Divider Circuit

1. Get the frequency range generated by the VCO
2. Get the Channel Spacing value i.e. S
3. Evaluate the 'Total division number N ' using

$$N = \frac{\text{Frequency Range of VCO}}{\text{Channel Spacing}} = \frac{f_1 - f_2}{S}$$
4. Get the value of Pre-Scaler i.e. P
5. Evaluate M using

$$M = \text{truncate} \left[\frac{N}{P} \right]$$
6. Evaluate A using

$$A = N - [M \times P] = N_1 \text{ to } N_2$$

[If the value of A is N_1 , the output frequency will be f_1 and if the value of A is N_2 then the output frequency will be f_2 . The range of A from N_1 to N_2 is for the desired output frequencies] .
7. End.

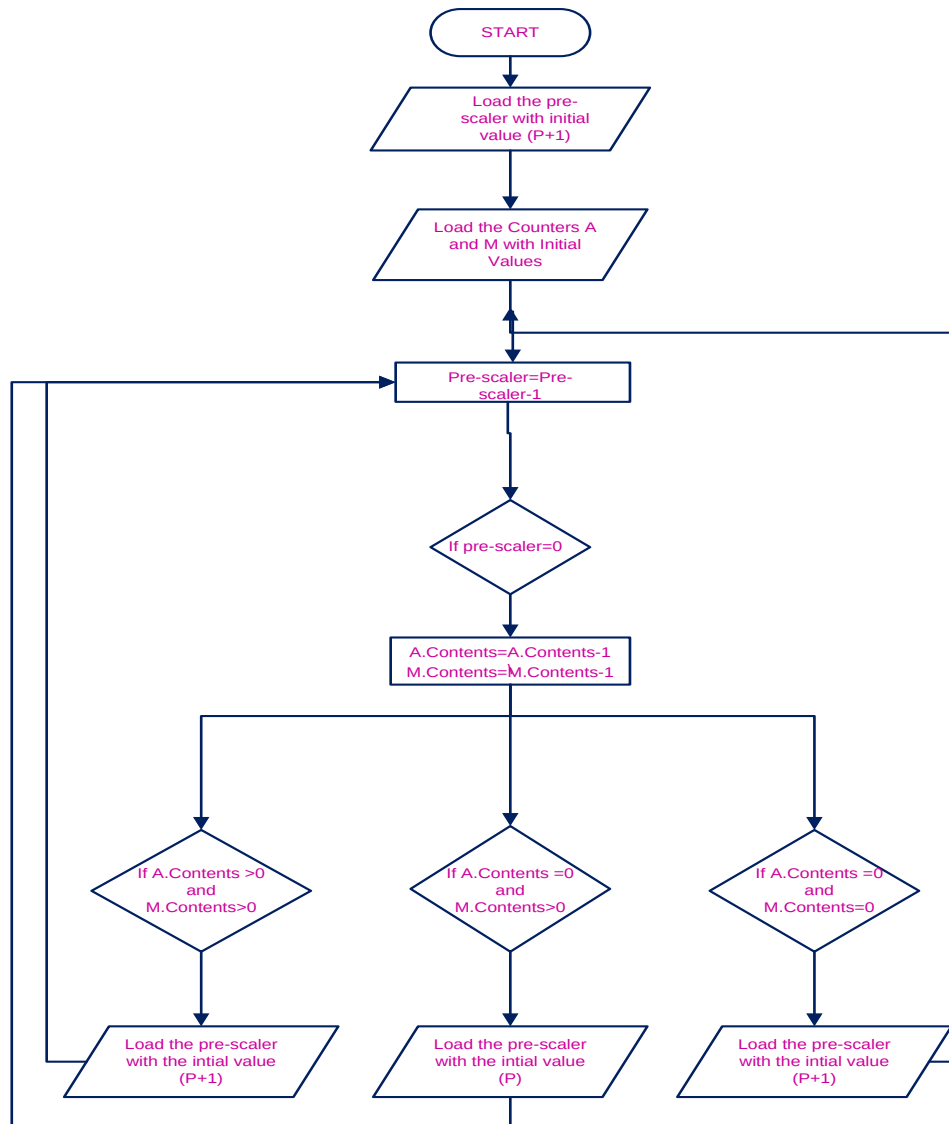


Fig. 2 : Flowchart for Two Modulus Loop Divider

iii) Design Of Prescaler

The pre-scaler shown in fig. 3 is comprised of JK flip flops. When the entire contents of pre-scaler become zero, the output 1 will go high and serves as the clock pulse trigger for the Swallow Counter (denoted by A) as well for the Main Counter (denoted by M) both of which are decrement counters as shown in the following figures. The clock pulse that is coming to the various flip flops of above pre-scaler is the output of high frequency VCO that has to be divided. The pre-scaler is kept loaded either with the value (P+1) or P. The Pre-scaler divides the frequency of VCO either by (P+1) or P and provides the divided (lower) frequency to A and M as the output of Pre-scaler (i.e. Output 1) is the clock signal for A as well for M.

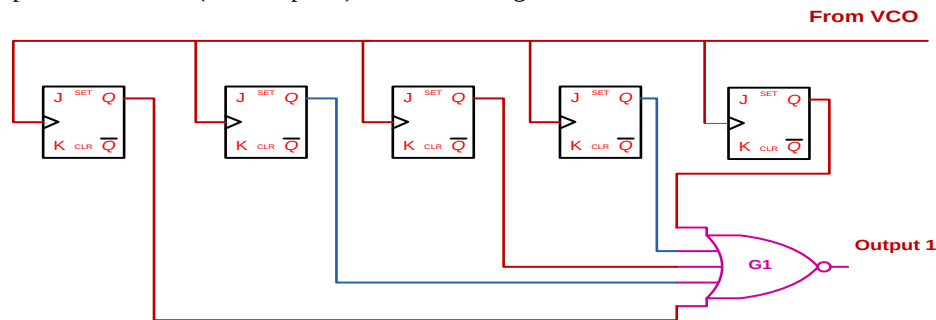


Fig. 3: Design of Prescaler

iv) Design of Swallow Counter and Main Counter

The Swallow Counter (A) (Fig 4) and Main Counter (Fig 5) are decrement counters comprised of JK flip flops. After (P+1) clock pulses, the contents of pre-scaler become zero. The moment the pre-scaler contents become zero, the contents of A as well as M get decremented by 1. The output 4 of G6 goes high and re-loads the pre-scaler with the value (P+1). Since the contents in the A are always kept less than M (as per algorithm), the A contents becomes zero prior to that of M contents. When the contents of A become zero, pre-scaler is re-loaded with the value P. Now only the M counter gets decremented by 1 when the pre-scaler contents become zero. When the contents of M counter also become zero (i.e. when both A and M attain zero), the control signal is sent to Phase detector, the pre-scaler is again loaded with the initial value (P+1) and the whole procedure starts again.

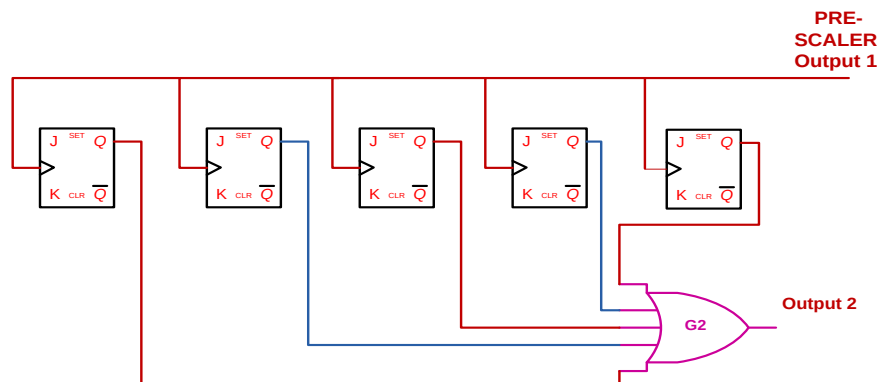


Fig. 4 : Swallow Counter Design

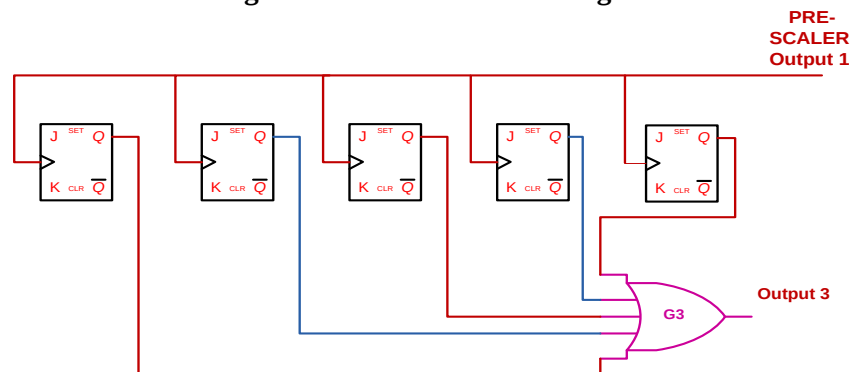


Fig. 5 : Main Counter Design

vi) Control Design

The designed control unit is used in figure 6. It comprises of two OR gates denoted by G4 and G5, three inverters and three AND gates denoted by G6, G7 and G8. The output 5 of G7 will load the pre-scaler with

value (P+1), the output 4 of G6 will re-load the pre-scaler with the value P and the output 6 of G8 will re-load the pre-scaler again with the value P.

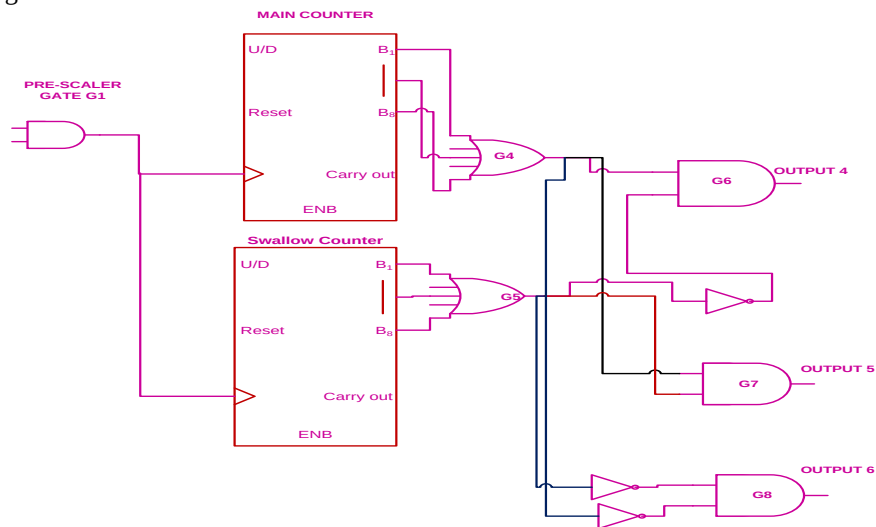


Fig. 6 : Control Logic Design

IV. Results and Discussions

In this paper the Lock Time has been evaluated by varying the value of resistance of the loop filter keeping other parameters constant and then by varying the value of zeta keeping other parameters constant. From the table 1, we can see that as we increase the value of R, the Lock Time increases and as we increase the value of Zeta, Lock Time decreases.

TABLE 1: Effect Of Resistance On Lock Time at C = 22pf

Resistance (K Ω)	Lock time (ns) at $\zeta = 0.6$	Lock Time (ns) at $\zeta = 0.7$
1.0	115	99
2.0	231	197
2.5	288	247
2.8	323	277
3.0	347	296
3.5	403	347

V. Conclusion

In this paper we describe the effect of loop filter resistance on lock time and obtain minimum lock time for a particular value of loop filter resistance. From table 1, we can see that as we increase the value of Resistance, the Lock Time increases and as we increase the value of zeta, the Lock Time decreases. The charge pump current is evaluated for different values of phase difference between the two pulses at the phase frequency detector and the corresponding control voltage generated at input of the VCO is also evaluated. It has been observed that as the phase difference is increased, the error voltage and thus the charge pump current also increases. This results an increase in the VCO control voltage.

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