



Analysis of Low Noise Amplifier in 3.1 to 10 GHz Range

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Abstract: A 3 to 10 GHz Low Noise Amplifier (LNA) with good gain and band pass property for Ultra Wide Band (UWB) applications using 0.18 μm CMOS technology is designed. Therefore, we proposed a wideband input network with band pass capability UWB LNA using LC network. It uses a CMOS amplifier with 0.18 μm technology. We have achieved A power gain of 49mW and minimum noise figure of 0.9 dB for the core LNA.

Index Terms: Complementary metal–oxide semiconductor (CMOS), low-noise amplifier (LNA), band pass, ultra wideband (UWB).

I. Introduction

The low noise amplifiers (LNA) are key components in the receiving end of the communication system and the performance is measured in a number of figures which are most notable while return loss, dynamic range and stability are examples of others. Signal received from the antenna is directly given to the low noise amplifier to reduce noise in external as well as internal noise of the circuit. In reference [1] there are used two MOSFETs in cascode topology which has little effects with each other. In this way, the device parameters of these two MOSFETs connected in cascode topology can be design separately, with almost no trade-off [2, 3]. This topology requires more area with complexity increment. References [4-6] presented that LNA which are able to provide gain to input signal powers up to -15 dBm without degrading linearity or adding much noise. These all properties enable the wireless receiver to operate in hostile communication environments. During the design of low noise, the most important factors are forward gain, low noise, matching and stability. In this paper, we design a CMOS LNA using single stage inductive source degeneration topology with respect to impedance matching and noise optimization. Generally the cascoded topologies are used in the designing of CMOS LNA. Here we have used the inductive degeneration common source topology with active device biasing. Active devices used to increase the temperature sensitivity. Major applications of the LNAs [7-9] are to increase the signal power as well as minimizing the noise. Reference [10] has proposed a model of the double-gate CMOS for double-pole four-throw RF switch design at nano meter technology, which is also an application for the LNA.

II. LNA Design Approach

The 3.1 to 10 GHz CMOS UWB LNA proposed here adopts a source-degenerated cascode configuration, as shown in Fig. 1. An LC input network for wideband operation is utilized with two new capacitors and for increasing the higher and lower band pass s, respectively. The load inductor in series with the resistor helps to enhance the gain flatness. The buffer transistor with a purely resistive load is employed for testing purposes. An additional inductor is inserted to enhance the overall gain. The overall gain of the LNA without an additional inductor L_c is given by [22] (L_c considered to be shorted)

$$= (1 + S_{11}) \frac{v'_{out}}{v_{in}} g_{m3(R_o || Z_o)} \quad (1)$$

$$S_{21} = \frac{(1 + S_{11}) v_{out}}{v_{in}}$$

Where

$$\frac{v'_{out}}{v_{in}} = \frac{g_{m1}(1 - \omega^2 L_g C_{RH})}{\square(\omega)} \left[(R_L + j\omega L_L) || \frac{1}{j\omega C_t} \right] \quad (2)$$

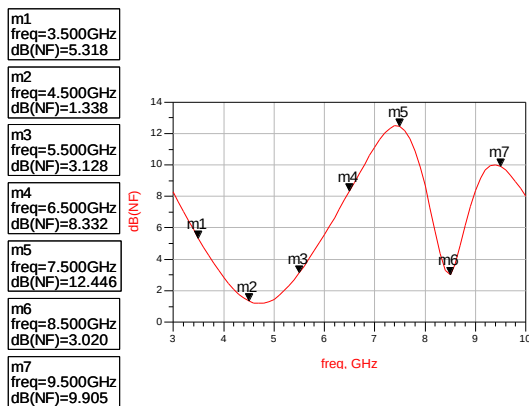
With

$$\square(\omega) = \omega^4 L_g L_s C_T C_{RH} - j\omega^3 L_g L_s g_{m1} C_{RH} - \omega^2 (L_g C_t + L_g C_{RH} + L_s C_t) + j\omega g_{m1} L_s + 1 \quad (3)$$

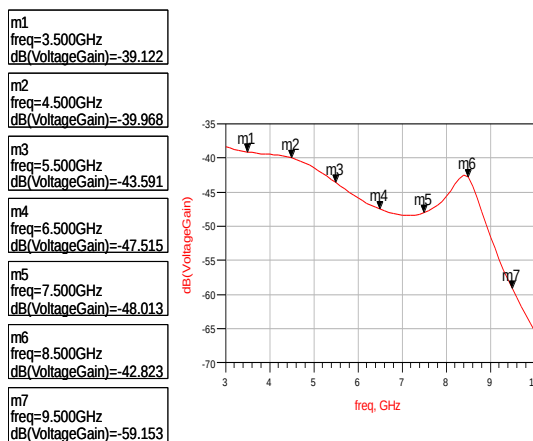
one parallel resonance from which the lower transmission zero can be created. It is expectable that a smaller impedance at the series resonant frequency will accomplish the superior out-band elimination efficiency.

III. Implementation and simulation

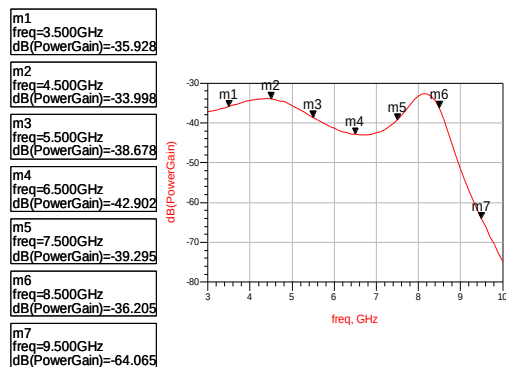
A. Noise Figure



B. Voltage Gain



C. Power Gain



Parameter / frequency	4.5GHz	5.5 GHz	6.5GHz
Noise figure	1.3 dB	3.1 dB	8.3 dB
Voltage gain	-39.97dB=10mV	-43.59dB=6mV	-47.51dB=4.2mV
Power gain	-33.99dB=19mW	-38.67dB=11.9mW	-42.90dB=7.16mW

IV. Conclusion

In this paper, we proposed a UWB LNA configuration with band pass ability and demonstrated the simulated results using the 0.18 μm CMOS process. Extra transmission zeros are created by the use of an *LC* input network with additional capacitors and for improving the higher and lower out-band performances. Finally we have achieved gain enhancement and low power dissipation with an additional inductor.

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