



A Review paper: A comprehensive study of Junctionless MOSFETs

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Abstract: All existing semiconductor junction transistors have reached the junctions 10nm channel length. For these difficulties in the semiconductor industry becomes challenging with the junction transistors. Therefore, the junctionless transistor is thought. They have added advantages in terms of low leakage current; less degrade mobility along with fabrication suitability. Variation of drain current with respect to drain bias and its analysis has based studies in various junctionless MOSFETs as worked out by the researchers.

Keywords: Double Gate Junctionless Transistor(DGJLT); Bulk Planner Junctionless Transistor(BPJLT);Duble Material Gate- Double Gate Junctionless Transistor(DMG-DGJLT);Gate All Around Junctionless Transistor(GAA JLT)

I. Introduction

The scaling of gate length in the bulk of MOSFETs decreases the efficiency of the gate control on the channel. In order to overcome limitation and ability to suppress short channel effects various device structures such as fully depleted SOI FETs and double gate and multiple gates FET have been proposed[2]. In such devices, however ultra-shallow source/drain junction fabrication is becoming one of the main required processing steps along with related thermal budget. However, the formation of ultra sharp junctions between source drain and channel becomes complex when the channel length of classical multigate MOS transistors is scaled down to extremely small dimensions. A solution to this problem in the form of novel structure called "Junctionless multi gate transistor"[2-5]. Junction less transistors have been considered as best candidate for the continuation of Moor's law and reduced electric field perpendicular to the channel[3]. Junctionless transistor can be described as a device which is heavily doped, and where the type of doping in the channel region is the same as source and drain regions. The device is fully turned on when operating at flatband condition, and turned off by full depletion of its channel region, whereby this depletion is caused by the work function difference between the gate material and doped channel region of the device. The lost gate control over the channel (charges) observed in very short channel transistors. For this problem gate alternative technologies, such as multi-gate architecture [6,7] can be thought. The presence of gate control on more than one side of the device effectively improves the electrostatic control over the channel, reducing short channel effects [1]. Especially the operation of JLT devices is quite different than the standard inversion (IM) transistors, on the contrary it is based on bulk conduction suspended to reduce surface roughness scattering. However, there are also several issues related to the channel doping and bulk mobility degradation and the variability of both threshold voltage and drain induced barrier lowering. The impact ionization occurs at the surface inversion layer in IM transistor but the bulk impact ionization occurs in the conduction channel in a JL transistor. Surface impact ionization occurs at the drain voltages ~ 40% higher than the bulk impact ionization; a large supply voltage is required for impact ionization in IM transistors [16].

The advantage of JL transistor also include: 1) lower leakage current 2) high I_{on}/I_{off} ratio 3) lesser sub threshold slope and variability[5]. However, it is difficult to fully deplete the channel region of JL transistor by utilizing the single gate control [3,4]. Use of high-k spacers or the combination of high and low-k spacers improves the devices on-state performance than the electrostatic integrity. JLTs operate at high vertical electric field in the channel in off state and low field in on-state. JLT transistors with high-k spacers can improves electrostatic integrity of the device and potentially making it scalable to extremely short channel length[15]. It was observed that the use of a high-k dielectric as a spacer brings an improvement in the off state current and the on-state current affected by dielectric constant of spacer. When increasing spacer width on-state current marginally decreases and off-state current marginally increases. Hydro-floro-oxides HfO_2 as spacer dielectric offer highest I_{on}/I_{off} ratio [12]. Dual material (DMG) devices offer improved carrier transport efficiency [21], transconductance and the drain output resistance compared with single-material-gate (SMG) conventional MOSFET [10-12]. Lou *et.al* have reported that in a DMG Junctionless Nanowire Transistor, out of different combination of L_{M1} & L_{M2} , $L_{M1}/L=1/2$ & work function difference=0.5 give overall best characteristics [13].Seung min Lee

et.al have reported that the impact of substrate bias, V_{BS} on the steep sub threshold slope in junctionless multiple gate MOSFETs has been analyzed experimentally [20]. Junction less nanowire field effect transistor such as the Gate-All-around architecture are potential candidates for next generation high speed and low power electron devices owing to their electrostatic integrity and simple fabrication steps, maintaining acceptable current densities[8],[32].The variability of the threshold voltage due to fluctuation of the channel dimension was reduced by increasing the number of gate electrodes coming into contact with each channel surface in multiple gate devices[23].

II. Junctionless Double Gate Field Effect Transistor

The main conduction mechanism in a junctionless Field-effect transistor (JLFET) relies not on the surface but on the bulk current; moreover, it turns off by making the channel fully depleted [1].Utilizing a single gate is rather difficult to fully deplete the channel, along with acceptable threshold voltage are also difficult to obtain under such condition [3]. Therefore, a double gate (DG) structure is a promising candidate for JLFETs due to its good electrostatic control of the channel [22].

Fig. 1 Schematic diagram of JL Double Gate (DG) MOSFET [22].

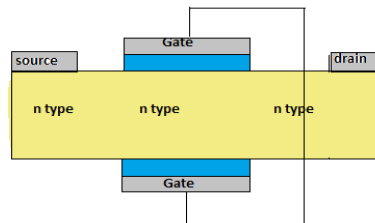
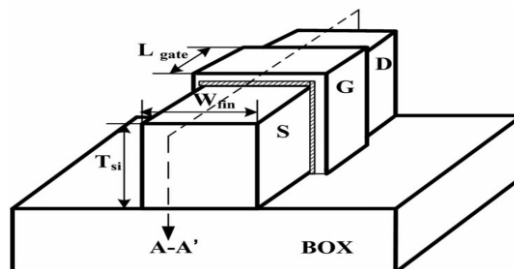


Fig.1 presents schematic view of Double gate of Junctionless transistor. This structure presents a real advantage since its fabrication process is simplified compared to the conventional process (there are no doping gradients in the device and no semiconductor type inversion). JL DG-FET characterized by a higher bipolar gain than IM-DGFET, due to stronger floating body effect has been discussed [27]. The main reason for low driving current in case of junctionless transistor is mainly due to the degraded electron mobility because of unavoidable high channel doping concentration [22]. The difference in electron velocity along the lateral position between conventional and junctionless DG-MOSFET with very low values of drain current in junctionless transistor compared to conventional transistor. The trans-conductance G_m of the junctionless nMOSFET is lower than that of conventional DG-MOSFET for the same gate voltage V_g . Junction less MOSFETs exhibits slower degradation of G_m compared to conventional MOSFET which can be well explained by the fact that the reduction in mobility with gate voltage [18]. *D.Munteanu et.al* shows that JL-DGFET SRAMs are naturally more immune to radiation than FDSOI SRAMs, but more sensitive to radiation than IM-DGFET SRAMs [28].

III .MULTIGATE JL FET

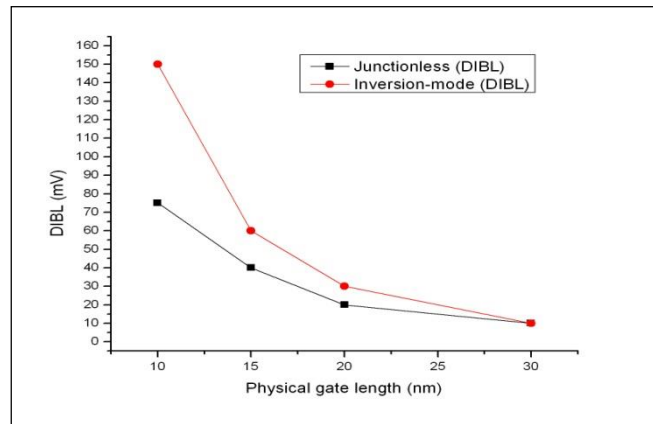
Fig.2 shows bird eye's view of a MuGFETs. The Simulated results for DIBL and threshold voltage versus physical length for both junctionless MuGFETs and inversion-mode MuGFETs are plotted in Fig.3.The junctionless MuGFETs have better short channel characteristics than inversion mode devices [6].

Fig. 2 3D View of gated resistor [6]



In a multigate FET the gate electrode is wrapped around a silicon wire, called finger or fin forming a gate structure that delivers optimal control.

Fig. 3 DIBL slope at $V_{DS}=50\text{mv}$ in junctionless & IM devices with $T_{si}=W_{si}=5\text{nm}$.[6]



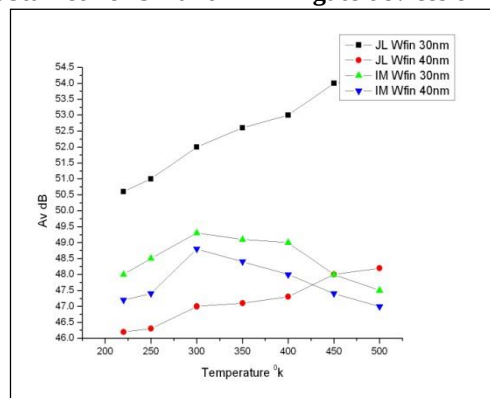
Channel is controlled electrostatically by the gate from multiple sides; channel is better controlled by the gate than conventional MOSFET. This provides greater voltage gain, which is useful for analog circuits. Multigate device is improved for on-state drive current to get fast circuit [11]. Early voltages V_{EA} and A_V are more sensitive to variation in W_{fin} for junction less devices than in inversion mode transistors. Junctionless transistors are able to provide a constant drain current over a wide temperature range. The different behavior observed between IM and JL devices as a function of temperature can be attributed to the lower variation of mobility with temperature in junctionless transistor [11]. In JL devices mobility almost independent of temperature. These effect explains the continuous increase in on current with temperature in JL MuGFET [24].

The influence of temperature on the intrinsic voltage gain of the device is addressed in Fig.4 for IM and JL devices with W_{fin} , mask of 30nm and 40nm of $V_{DS}=1\text{V}$. IM devices present maximum gain at room temperature, whereas A_V always increases with T in JL transistor [7].

IV BULK PLANNER JUNCTIONLESS TRANSISTOR

The bulk planner junctionless transistor (BPJLT) is a source-drain-junction free transistor accompanied with junction isolation.

Fig. 4 A_v versus T obtained for JL and IM Tri gate devices of $L=1\mu\text{m}$ at $V_{DS}=1\text{V}$.[7]



It is junctionless in the source-channel-drain path but needs a junction for vertical direction for isolation purpose. The advantage of BPJLT over existing transistor are i) The full compatibility to industry standard ii) Lower cost iii) Better scalability. The device is advantageous for low thermal budget on gate formation [29].

Fig. 5 Schematic representation of bulk planner and SOI junction less n-channel transistor.[29]

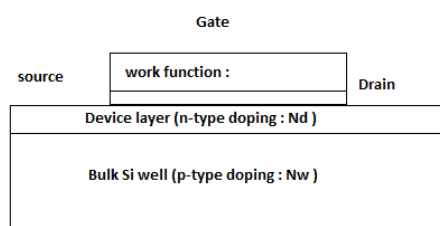


Fig.5 shows that the BPJLT device architecture for n-channel operation. A thin n type “device layer” is formed on p-type silicon. A gate stacks with a gate dielectric and gate metal of work function of 5.1eV is formed on top of the n type layer. The dielectric isolation used in SOI architecture is replaced by junction isolation in BPJLT [29]. BPJLT has uniform lateral doping i.e. the source, drain and the channel has identical doping. In the on state, the SOI-JLT device is uniformly doped in flat-band, whereas for the BPJLT a fraction of the device layer at the top-corresponding to the effective device layer (in flatband) the rest remains depleted [29]. The thinner effect is in the case of the BPJLT that it would exhibit better electrostatic integrity than the SOI-JLT. BPJLT has superior I_{ON}/I_{OFF} , smaller drain-induced-barrier-lowering (DIBL) and subthreshold slope. This establishes the superior electrostatic integrity. Device with high-k spacer [15] shows a reduced off-state leakage current. As the dielectric constant of spacer increases, the slope of the plot I_D versus V_{GS} increases by using appropriate gate metal work function, the improved gain in the leakage current can be traded for higher ON current in the device using high-k spacers. The junction isolation of BPJLT would however come with a capacitance that could increase the delay of operation [29].

III. NANOSCALE JUNCTIONLESS DG MOSFET WITH DUAL MATERIAL GATE STACK

Fig.6 shows that Junctionless Dual Material Double Gate (JLDMDG) MOSFET. The channel central electric field distribution versus the channel length for JLDMDG MOSFETs and JLSMDG MOSFETs is shown in Fig.7. JLDMDG MOSFETs have gate length ratios of $L_1:L_2=1:2$, $L_1:L_2=1:1$, and $L_1:L_2=2:1$. It is observed that there is an electrical field peak period which can provide more acceleration to electrons in the channel and improve the efficiency of carrier transportation [17].

Fig. 6 Schematic cross sectional view of JLDMDG MOSFETs, the gate near the source region is denoted as a control gate and the gate near the drain region is denoted as screen gate [17]

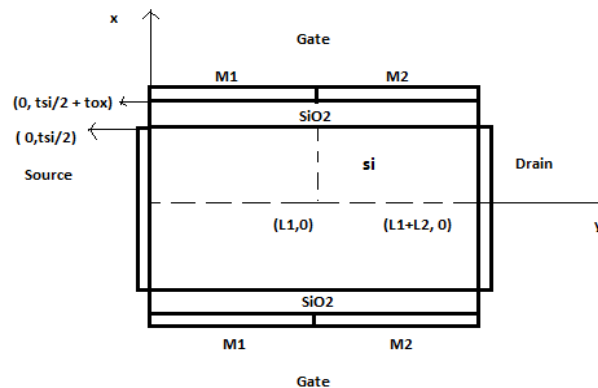
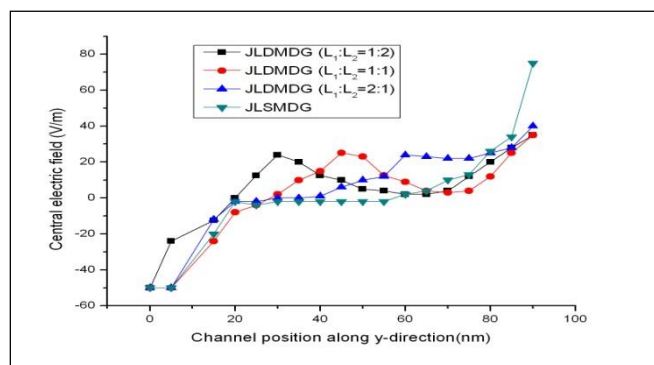


Fig.7 the simulation results of the JLDMDG MOSFETs are compared with those of the JLSMDG MOSFETs. The simulated device parameters are $t_{Si}=15nm$, $t_{ox}=1.5nm$, $L=90nm$, and $V_{gs}=0V$. [17]



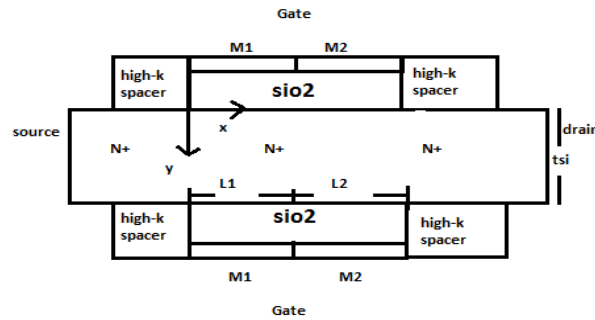
The variation of the electric field at the drain end of JLDMDG MOSFETs is much smaller than that of JLSMDG MOSFETs as the drain bias increases. The electric field distributions of the JLDMDG MOSFETs ensure better average electric field across the channel and suppress the Hot Carrier Effect (HCE) by the high drain voltage [17]. The potential distribution of a DMG-JNT has suddenly changed near the transition of the two gates, whereas that of SMG-JNT increases monotonically from source to drain. The sudden change is caused by the difference of gate work function and enhance the electric field in the channel of the DMG-JNT [13].

Potential drop across the source/drain extension in the DMG-JNT is larger than that of SMG-JNT, which indicates that the channel on-state resistance of DMG-JNT is smaller than that of SMG-JNT [10]. The electron velocity in the DMG-JNT can be increased to three times of that of the SMG-JNT at the same location. The transconductance g_m of the DMG-JNT in the saturation region is higher than that of SMG devices [13].

IV. DUAL MATERIAL GATE JUNCTIONLESS TRANSISTOR WITH HIGH-K SPACER

The device structure for an n-type symmetric DMG-SP DGJLT is shown in Fig.7. Drain current for the devices at a drain voltage of 50mV in linear scale. High-K spacer enhances the fringing electric field through the spacer and depletes the silicon beyond the gate edges in the off state, which improves sub-threshold characteristics [16]. Out of different combinations of gate oxide/spacer dielectric material considered (namely SiO_2 , Al_2O_3 , and HfO_2), SiO_2 as gate oxide and HfO_2 as spacer dielectric offer highest $I_{\text{ON}}/I_{\text{OFF}}$ ratio [30]. Current characteristic of Dual Material Gate Junctionless Nanowire Transistor (DMG-JNT) with different ratio of L_1/L . Shown in Fig.8 drain current I_D with respect to drain voltage for the devices at $V_{\text{GS}}=1\text{V}$.

Fig. 7 Cross sectional view of an n type DMG-SP DGJLT [16].



The DMG-SP has higher output current followed by DMG and SMG DGJLT due to high fringing electric field. High-K spacer is incorporated in a DMG symmetric DGJLT architecture forming DMG-SP DGJLT. DMG-SP offers superior transconductance compared with DMG and SMG DGJLT [16]. All the capacitances are extracted from the small-signal ac device simulations at a frequency of 1-MHz. The DMG-SP has highest C_g compared with DMG and SMG-DG JLT [16].

It should be noted that ratio=0 and ratio=1 corresponding to the Single Material Gate Junctionless Nanowire Transistor (SMG-JNT) cases with gate work function of 4.27eV and 4.97eV, respectively. As shown in Fig. 9, I_{OFF} decreases with increasing L_1 . In addition the effect of V_{DS} on I_{OFF} also decreases with increasing ratio of L_1/L . It is because the increasing L_1 leads to more depletion charge at the same gate voltage.

Fig. 8 Output current with respect to drain voltage at $V_{\text{GS}}=1\text{V}$ for $L=40\text{nm}$, $T_{\text{si}}=10\text{nm}$, and $T_{\text{ox}}=1\text{nm}$ [16]

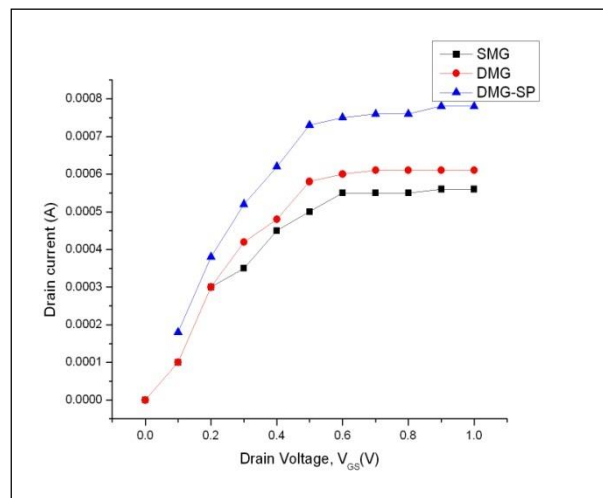
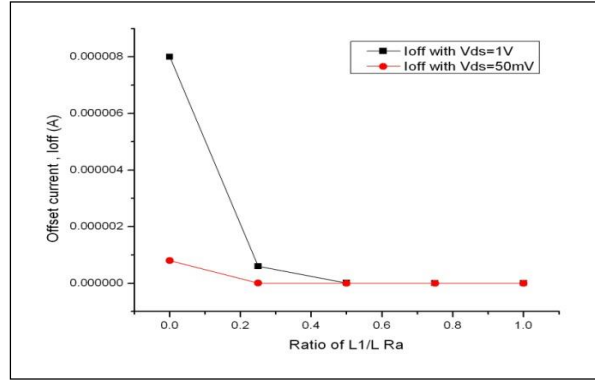


Fig. 9 Variation of off state current [16]



The peak value of the electric field near the drain of the Dual material Gate junctionless Nanowire Transistor is reduced by 40% compared with that of Single Material Gate Junctionless Nanowire Transistor [13]. The DMG structure is more effective in reducing the drain channel field, which in turn suppresses the short channel effects and the hot carrier effect in Junctionless nanowire Transistors [13].

V. Gate -All- Around Junctionless Transistor

Fig.10 shows that Schematic representation Gate-All-Around (GAA) Junctionless transistor [23]. The Gate-All-Around junctionless transistor devices showed excellent characteristics with the aid of the GAA and junction free nature. The variability of the threshold voltage due to fluctuation of the channel dimension was reduced by increasing the number of gate electrodes coming into contact with each channel surface in multiple gate devices [23].

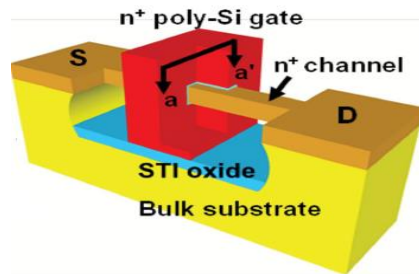


Fig. 10 Schematic representation Gate-All-Around Junctionless transistor. [23]

The typical transfer and output characteristics of the fabricated All-Around-Gate (AAG) junctionless transistor with the oxide/nitride/oxide gate dielectric. The transfer characteristics shows good dc performance levels with an on/off ratio that exceeds 10^5 and good gate controllability even with an EOT of 13nm, $L_G=50$ nm. The sub-threshold swing (SS) of the AAG junctionless transistor is approximately 130mV/decade [25]. However, scaled Nanowires typically suffers from parasitic S/D resistance, which can be mitigated by taking advantage of the high electron mobility and versatile band gap & doping engineering of III-V materials. The fabricated short channel ($L_G=80$ nm) GaAs Gate-All-Around (GAA) Nanowire MOSFETs (NWFETs) with extremely scaled NW width ($W_{NM}=9$ nm) exhibits excellent g_m linearity at biases as low as 300mV. The high linearity is insensitive to the bias conditions, which is favorable for low power applications [26].

Table 1: Comparison of Junctionless AND Inversion Mode Transistor

Sr. No.	Junction less Transistor	Inversion Mode MOSFET
1	Junction less MOSFETs has extremely low leakage current and simple fabrication processes.	Conventional MOSFET more leakage current and complex fabrication process.
2	Electric field perpendicular to the current flow is found to be significantly lower in junction less transistor.	Inversion channel mobility in metal oxide semiconductor transistor is reduced by this electric field.
3	Bulk conduction of junction less transistor is credited for reduced surface roughness scattering.	In inversion mode transistor reduce mobility of electron due to surface roughness scattering.
4	Current drive of JL MuGFETs increases with temperature (Mobility remains constant with Temperature)	Current drive of IM MuGFETs decreases with temperature (Mobility decreases with increasing temperature).
5	JL DG FET characterized by a higher bipolar gain than IM DG FET.	IM DG FET lower bipolar gain compared to JL DG FET.
6	Junctionless MOSFET slower degradation of G_m for high gate voltage	IM MOSFET high degradation of G_m compared to junctionless MOSFET.
7	Lower S/D series resistance is also found in JL device.	Maximum S/D series resistance compare to JL device.

VIII. CONCLUSION

The objectives of this review paper to discuss the junctionless device technology and analyze the findings having material approach.

The findings are:

- In junctionless transistor the I_{ON}/I_{OFF} , DIBL and sub threshold slope are improved with higher spacer dielectric constant. With increasing spacer dielectric constant sub threshold slope decreases.
- Junctionless MOSFET exhibits slower degradation of G_m compared to conventional MOSFET.
- The work function difference significantly affects the characteristics of devices by changing the channel control ability and the screening effect.
- Junctionless transistor is able to provide a constant drain current over wide temperature range, unlike IM device.
- The variability of the threshold voltage due to fluctuation of the channel dimension was reduced by increased by increasing the no of gate electrodes coming into contact with each channel surface in multiple gate devices.

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