



Carbon Nano Scale FET's and CMOS Technology – A REVIEW

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Abstract: Gordon Moore had led us to this great concept of doubling the transistors on the single chip after every 18 months which in turn left us with high density chips. The CMOS technology evolved where we can work at even deeper submicron levels. But as the technology shrunk the secondary effects in the CMOS plays their part and to use CMOS at around 22nm becomes difficult as the device performance variations also come into existence. To overcome all these secondary effects CNT's are used. These are cylindrical hollow structural tubes which belong to the family of graphene. These CNT's are used as a bulk material in CNTFET, which make these FET's to work at deeper sub-micron levels without any device performance variations.

Keywords: CNT (Carbon Nano Tubes), CNTFET (Carbon Nano Tube Field Effect Transistor), CMOS, Nano scale.

I. INTRODUCTION

In 1963 Gordon Moore predicted that because of the continuous miniaturization, transistor count on the same chip would double itself in every 18 months. [1] And actually his prediction turned true and now it is being treated as a law. As reduction in the size of transistors leads to increased speed and decrease in area. However, with the advancement in technology the device kept on scaling which in turn resulted in high circuit density and increased performance by about 40% in every technology generation, followed by "Moore's Law," [1, 2]

Such an advancement has let transistors to become smaller and faster, which in turns consume less power, and are cheaper to fabricate. As transistors cannot be smaller than that of an atom hence the scaling cannot go on forever. The first integrated circuit which arrived in the market was fabricated using bipolar technology which was made up by using few 100 transistors. Even though the principles were well known, but MOSFET arrived in the market several years later. One of the reasons behind the late arrival of the MOS was its inherent instability, as its gate dielectric consists some minute amount of alkali element which could cause the shift in the threshold voltage of the transistor during its operation.

However, in bipolar circuits the problems of high power consumption became prominent enough. Even when all transistors are switched 'OFF', the sum of the leakage current in bipolar transistors is fairly large. The solution to this problem was MOS technology which eventually made its way [3]. To scale down the dimensions of MOS devices is easier than any other transistor technology. [3, 4, 5]

MOS technology got evolved and in eighties, CMOS processes were widely adopted. Present day integrated circuits would never have been existed if the CMOS

Technology would not have been accepted and implemented around the late eighties. High noise immunity and low static power consumption are two of the most important characteristics of CMOS devices. In case of CMOS significant power is only drawn when CMOS device are switching between on and off states. Resulting, CMOS devices produces less heat than any other technology. [4]

Now the advancements have led to the research of nanoscale devices. The nanoscale Devices and Systems deals with the devices structures with characteristic sizes of ~100nm and below, at such a low sizes phenomena such as quantum confinement and single-electron effects in electronics, near-field behavior in optics and electromagnetics, single-domain effects in magnetism etc. have become dominant. [3]

As working on this Nano scale technology there are a number of Nano electronic devices that can become a possible supplement or replacements of current CMOS devices. These Nano electric devices include nanowire or carbon nanotube transistors, graphene FETs, single electron transistors, and spin transistors.[5] Out of all these nano electronic devices CNT FET's will be discussed in this paper, which uses carbon nano tubes as it bulk channel material in place of silicon which is being used in the traditional CMOS technology. These FET's have a good control over channel formation, it has a better threshold voltage, improved sub threshold slope, High electron mobility, High current density and High trans conductance.

II. CMOS TECHNOLOGY OVERVIEW

CMOS is abbreviated as Complementary Metal Oxide Semiconductor. The words "complementary-symmetry" refers to the typical design style of CMOS as it uses complementary and symmetrical pairs of p-type MOSFET and n-type MOSFET for implementation of any logic functions. [7]

High noise immunity and low static power consumption are two important characteristics of CMOS devices. The series combination draws significant power only momentarily during switching between on and off states as Since one transistor of the pair is always off, in result to this, CMOS devices produce less amount of heat than any other logics. Hence less heat is wasted as like transistor–transistor logic (TTL) or NMOS logic. Also these logics have some standing current even when the device is not changing its state. Due to CMOS technology a large density of logic can be implemented on the same chip. This has been one of the most important and unique reasons that CMOS became the most used technology to be implemented in VLSI chips.

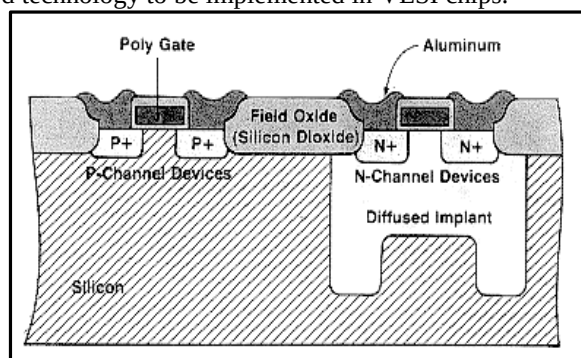


Figure 1: A Cross Sectional View of CMOS

Since there is never a purely resistive path to ground hence it consumes no DC power. The device has a symmetric output because the pull-up and pull-down resistances of the P- and N-channel transistors are made same. The fabrication of CMOS is quite difficult than that of NMOS as in CMOS since two different types of transistors are made on the same substrate as shown in figure 1. Figure 2 shows a set of transient output characteristics for a typical CMOS inverter. In this example the NMOS pull-down transistor has the minimum channel length and width of 3μ , while the PMOS pull-up transistor has a channel width of 6μ . The output load for the inverter is another identical inverter, and the input is a pulse with a 0.5 n [4, 7]

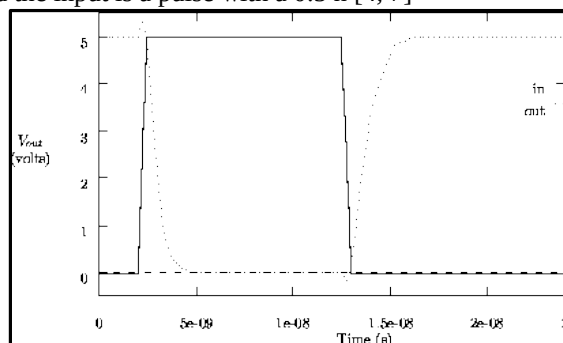


Figure 2: Transient Output for a Typical CMOS Inverter

CMOS technology is said to be the cheapest of all the available technologies having the same feature size. Circuit designing in CMOS technology is supported by many resources. CMOS technology can be further scaled down as per the technology. [7] It draws a very little amount of power at low frequency. CMOS technology can make mixed signals (digital and analog) together on a single chip and this technology can integrate large number of transistors on the same chip. On the other hand it consumes a lot of power at high frequency and it has low trans conductance than BJT. [7, 8] More over if the switch of a CMOS inverter is kept on for a long time then it can be damaged easily. There is large lump capacitance in CMOS which leads to large propagation delay than any other logic families. The noise margin in CMOS are also low. [7, 9]

III. CHALLENGES WITH NANOSCALE MOSFETs

To have detailed study about the phenomena that occurs in nanoscale MOSFET's leads us to provide useful interpretation of the anomalies that we might encounter in their SPICE simulations, along with this it also provides us the future possibilities and limitations of the device scaling. In the following section, we will stress on these phenomena. We will start with a brief overview of scaling trend of silicon-based planar bulk MOSFETs and highlight the challenges to be solved. Current approaches to control

these small-geometry effects such as increased leakage currents, threshold voltage variations, weakened gate controllability over the channel, and increased in S/D resistances will be discussed.[7]

IV. CARBON NANO TUBES FET

Carbon nanotubes (CNTs) were discovered in 1991, these are allotropes of carbon which have a cylindrical structure, the length-to-diameter ratio of nano tubes is up to 132,000,000:1 hence they are cylindrical nanostructures, These cylindrical carbon molecules have very unique properties [10], the thermal conductivities of CNTs is extraordinary and mechanical and electrical properties which make them very important for nanotechnology, Carbon Nano tubes are used in many areas like electronics, optics and other fields of materials science and technology.

Carbon Nano tubes actually belong to the fullerene family and their name is inspired by their long and hollow structure whose walls are formed by one atom thick sheets of carbon, called graphene.

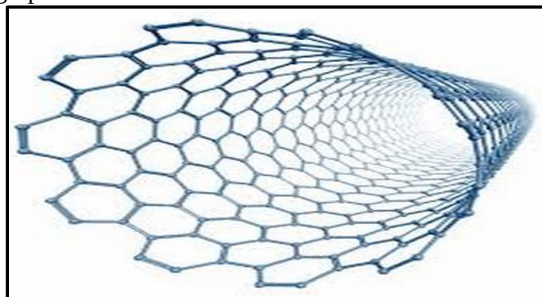


Figure 3: Cylindrical Carbon Nano Tube

These carbon nanotubes can be of metals or semiconductors depending upon the method on which it is rolled. These sheets are rolled at specific and discrete angles, which are called as chiral. And the combo rolling angle and radius decides the nanotube properties. The way CNT's are rolled is called its chirality. There is an advantage with the nanotubes that their threshold voltage can be easily controlled. The band gap of CNT and their diameter are inversely proportional to each other so either can be controlled by varying the other. Band gap of CNT's are inversely proportional to their diameters. [7, 10].

The Carbon Nano tubes have great strength precisely due to the nature of bonds they inherit. The chemical bonding of nanotubes is composed entirely of sp^2 bonds, which is same as that found in graphite. These sp^2 bonds are stronger than the sp^3 bonds which are generally found in alkanes and diamond. Due to the qualities like have high thermal conductivity, current carrying capacity, and excellent mechanical and thermal stability nanotubes can be used as interconnects in the future. [11] now importantly these CNT's are used in CNTFET (carbon nanotube field-effect transistor), these transistors use CNT's as the channel material instead of silicon which is used in routine CMOS technology. CNTFET have a single carbon nanotube or an array of carbon nanotubes as the channel material.

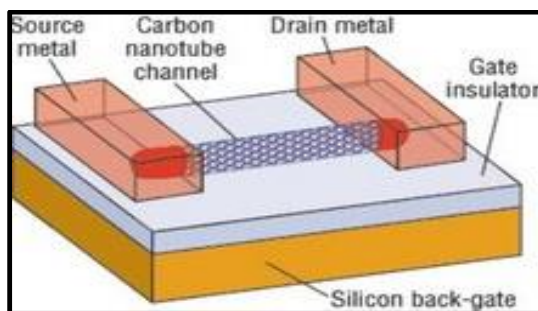


Figure 4: A CNTFET, With Carbon Nanotube as Channel Material

Now the challenges come into existence when the technology goes to 22nm and so. At this very channel length fabrication and device performance issues comes into picture. [12] When we talk about CMOS technology there are a number of limitations that a device has to face as the technology shrunk, few of the, electron tunneling through short channels and thin insulator films, variations in device structure and doping, leakage currents, passive power dissipation, short channel effects etc. [13] These secondary effects can be reduced by using CNT's as channel material, where one of the ways is to use CNTFET's. one of the greatest feature in Carbon Nano tube is that there is no boundary scattering because of the lack of boundaries in the perfect and hollow cylinder structure of CNTs. CNT's allow only forward and back ward scattering as the material they use is quasi-1D. These properties make CNT a reliable material to be used in future. [14] Due to the strong covalent carbon-carbon bonding, with sp^2 configuration, makes carbon nanotubes chemically inert. Also carbon nanotubes are able to transport large amounts of electric current. Carbon nanotubes are also able to conduct heat nearly as well as diamond or sapphire, and due to their miniaturized dimensions, the CNTFET uses much less power than a silicon-based device and have high speeds [15].

V. CONCLUSION

CNT's are inert in nature due to the bonding arrangement and nature of bonds. It has high thermal conductivity, current carrying capacity, and excellent mechanical and thermal stability, hence CNTFET's can face different fabrications and device challenges, like electron tunneling through short channels and thin insulator films, variations in the structure of device and doping, leakage currents, passive power dissipation, short channel effects etc., than CMOS where simple silicon is used as a bulk material.

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