



Design of High Performance and Energy Efficient Domino Logic

Shilpa Sharma¹, Manish Kansal²

¹M.Tech. Student, ²Head of Department,

^{1,2}Department of Electronics and Communication,
Panchkula Engineering College, Panchkula, Haryana, INDIA.

Abstract: Domino Logic circuit is the extended part of the Dynamic Logic. This paper reduces the problem associated with the design of Dynamic logic. Charge sharing and charge leakage is the main drawback of dynamic logic circuits. In This paper a design a new domino logic design is proposed. This proposed domino logic shows reduced power delay product at 1V supply Voltage and IBM 90 nm CMOS technology. This domino logic has simulated for the case domino OR logic.

Keywords: Domino Logic, Charge Sharing, Leakage Current, Dynamic Logic.

I. Introduction

The invention of transistor brought about a giant technology leap in microelectronics. With the advent of transistor and the arrival of IC's, power dissipation is a lesser concern. Greater emphasis is placed on performance and size. To continue to improve the performance of circuits and to integrate more functions into chip, feature size reduces significantly. As a result, the magnitude of power per unit area (power density) has kept growing and the problem of heat removal and cooling getting worse. In the last few years we have seen that the emerging battery powered portable applications like pocket calculator, hearing aids, implantable pacemakers should consume less power for longer life. Consequently, ever since then power reduction has become one of the most critical factors in the evolution of technology. Even with the scaling of supply voltages power dissipation has not reduced significantly because more number of functionality is embedded in a single chip. An alternative to solve this problem could mean accepting either the large cost for cooling subsystem. Ineffective cooling degrades reliability. As a result today it is widely accepted that power efficiency is another important design criteria along with area and performance. So the power consumption should be minimized at each abstraction level and at each phase of the design process. The domino logic structure is similar to that of dynamic logic along with a static CMOS inverter is used to avoid cascading problem as shown in Figure 1. During precharge phase (CLK=0), the output of dynamic logic is charges to VDD and the output of inverter is become zero. During evaluation phase (CLK=1), the node OUT makes only transition from 0 to 1. Since in the precharge phase the node OUT discharges to logic 0, hence the false evaluation is avoided during cascading of various domino blocks. As it uses static inverter only non-inverting logic can be realized and it increases propagation delay.

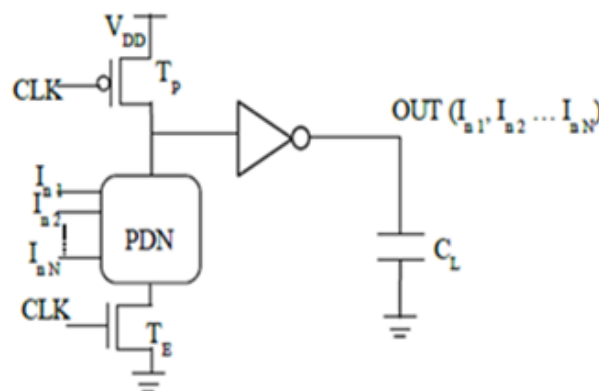


Fig 1: Domino CMOS Logic

In this paper we have proposed a new domino logic circuit scheme for improving power-delay product. The remaining paper is organized as follows. Section II presents the drawback of the conventional CMOS domino Logic. Section III presents an overview of the previous domino logic designs. Section IV presents new modified domino logic circuit design. The comparison and the results and their analysis have given in section V, finally the sections VI presents the conclusion.

II. Drawback of Conventional CMOS Domino Logic

Some problems of CMOS dynamic and Domino logic are charge sharing and charge leakage problem.

Charge Leakage: The operation of the dynamic CMOS logic style gates are based on the pre-charge of the capacitor at the output of the gate. The capacitor charged has to remain on its state during all the evaluate phase if the PDN network is off. Due to the leakage currents in the circuit, that capacitor start discharging and if it reaches a voltage level lower than the allowed by the noise margins, the gate will have a malfunctioning behavior.

Charge Sharing: Other issue in the dynamic logic style gates is charge sharing. Take as an example the Figure 2 and assume that initially all capacitances are discharged and that all inputs are set to zero during the pre-charge. Then, during the pre-charge phase, the output capacitance has to be charged again. If the inputs make transitions from zero to one, the charge is distributed with the internal capacitances. This causes the voltage of the output node to drop and may result in an inconsistent behavior of the logic gate.

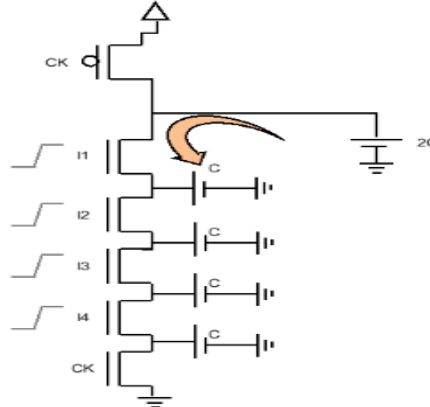


Fig 2: Charge sharing in 4 input NAND gate

III. Overview of Previous Work

The previous domino logic is shown in figure 3. Shiksha et al have proposed the design using the concept of current mirror. They have used the current mirror in stack. The purpose of the current mirror in this circuit is to reduce the leakage current to the ground via M4 and M5 transistor. They uses the conventional effect of stacking, these stack of transistor in pull down network reduces the power dissipation as well as the delay of the circuit. The size of the pull down network is also increases.

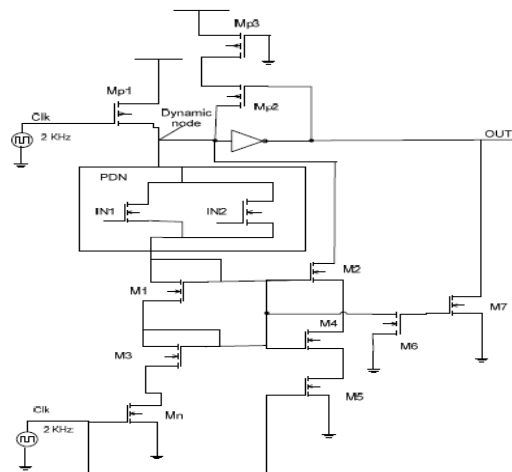


Fig 3: Shiksha et al. Domino Logic circuit for OR gate [1]

IV. Modified Domino Logic Scheme

The modified circuit of domino logic contains the PMOS transistor in footer logic, the schematic and configuration of this approach work in a manner so it can reduce the leakage to ground and indirectly reduces the power dissipation novel low-leakage-power design is described. The transistors are held in reverse body bias. This reverse body biasing increases their threshold. This increased threshold voltage results in low leakage current and hence low leakage power. As we know the leakage current is the main causes of power dissipation we have reduce the leakage power using a PMOS transistor in Footer circuits. The Modified design has shown in figure 4. PMOS degrades the low logic level. As we know that static power is relative to the voltage apply, through the reduced voltage the power decreases and we get the advantage of less degradation of logic. This

approach contains another advantage during off mode if we increase the threshold voltage PMOS Transistors in Footer Circuits. The transistors are held in reverse body bias. Because as result their threshold is high, higher threshold voltage causes low leakage current and therefore low leakage power. If we use minimum size of transistors, i.e. aspect ratio of 1, we yet again get low leakage power due to low leakage current. As a result of stacking, PMOS footer transistor will get less drain voltage.

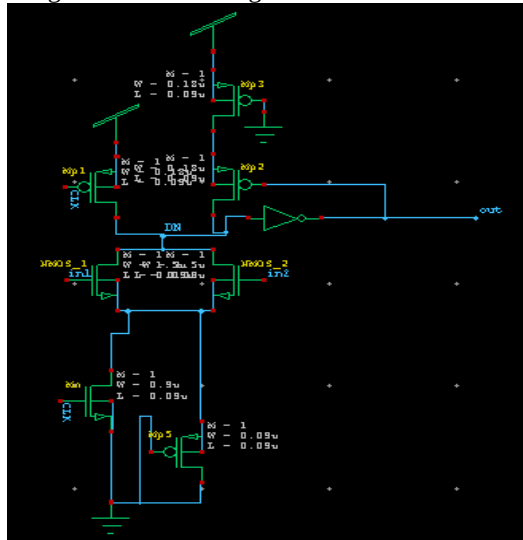


Fig 4: Modified Domino Logic Circuit Design

V. Results and Analysis

The simulation of Modified Domino Logic. This high speed Domino Logic structure different in design, it contains an indirect path to the ground. The pull down network is design using a PMOS and NMOS transistor in parallel. These all structures works in two modes one is precharge phase and other one is evaluation phase.

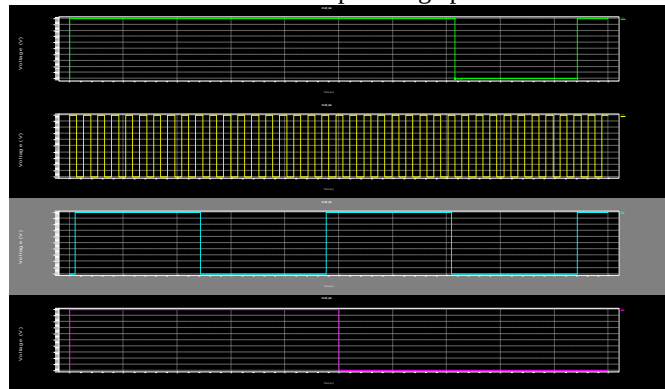


Fig 5: Output waveform for Low PDP Modified Domino Logic.

Its output behavior shown in the figure 5 which shows that the circuit works well in evaluation phase for the OR dynamic Logic. The switching time of the proposed circuit makes it a high speed and low power consumption circuit. All simulation of the proposed and existing circuit has been performed at 90 nm technology with 1V supply voltage. The all circuits have been tested on same input condition for a perfect combination of comparative analysis. In the table 1 we have given the result of different simulated Domino techniques. This circuit has also been simulated for different supply voltages. To do this there has been applied a voltage sweep from 1V to 0.5V. The comparisons of the proposed modified design with previous design have been shown in further tables.

Table 1 Power, Dealy and Power Delay product Comparision of Previous and Modified Design

Different Domino Logic Designs	Basic Domino Logic	Footless Domino Logic	Footer Domino Logic	Previous Domino Logic	Modified Domino Logic
Supply Voltage(V)	1	1	1	1	1
Power(μ W)	13.3	78.4	3.19	0.074	0.063
Delay($\times 10^{-20}$)	338	155	103	2.55	0.635
PDP($\times 10^{-19}$)	4495.4	12152	328.5	118.3	40.004

Table 2 Modified Design Power Delay Products with Different Supply Voltages

Supply Voltage(V)	1	0.9	0.8	0.7	0.6
Power(μ W)	0.063	0.048	0.035	0.026	0.019
Delay($\times 10^{-10}$)	0.635	0.709	0.911	1.292	2.275
PDP($\times 10^{-19}$)	40.0	34.0	31.9	33.6	43.2

To do the more accurate analysis of proposed design there has been done a simulation on different width of the extra PMOS transistor in Pull down Network; the width sweep is taken from 90 nm to 540 nm.

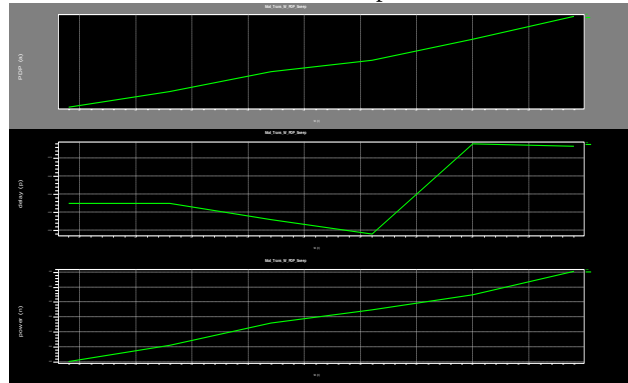


Fig 6: Output power and delay for modified Domino at 90nm to 540nm Mp5 Transistor width sweep.

The graphical representation of the proposed work describes the decrement of the PDP with the decrement of Mp5 transistor width.

VI. Conclusion

In The proposed work there have been designed and simulated different Domino logic circuits like Footless Domino Logic, Footer Domino Logic, Shiksha et al. Domino Logic and Modified Domino. These logic cells have been designed and simulated on 90 nm IBM fab file using MOSIS Test Data. The whole simulation of this Domino technique for these different designs have been done using Tanner EDA environment. The proposed Domino logic circuit is found to give better performance than the previous design. It has been tested to have better power supply sustainability and significantly less power and power-delay product at various power supply voltages. Domino logic circuits have a marginal increase in area compared to the CMOS circuit; overall, there has been achieved the lower power dissipation with proposed technique.

References

- [1] A.Devgan, "Efficient couple noise estimation for on-chip interconnects", ICCAD97, pp. 147-151, 1997.
- [2] K.S. Yeo, K. Roy, 'Low- Voltage, Low-Power VLSI Subsystems'.
- [3] K. Roy, S. Prasad, 'Low-Power CMOS VLSI Circuit design', a willey Interscience Publication, 2000.
- [4] A.P. Chandrakasan and R.W. Broderson, 'Low Power Digital CMOS Design,' Kluwer Academic, 1995.
- [5] Mohamed I.Elmarys and AbdellatifBellaouar, "Low-Power digital VLSI Design Circuits and Systems", Kluwer Academic, 1995.
- [8] G. Balamurugan and N. R. shanbhag, "The twin-transistor noise tolerant dynamic circuit technique," IEEE J. Solid-State Circuits, vol. 36, no. 2, pp. 273-280, Feb. 2001.
- [9] K. L. Shepard and V. Narayanan, "Noise in deep submicron digital design," in Proc. ICCAD, pp. 524-531, 1996.
- [10] K. L. shepard, "Design methodologies for noise in digital integrated circuits," in Proc. DAC', pp. 94-99, 1998.
- [11] C. Murthy, "Process variation effects on circuit performance: TCAD simulation of 256-Mbit technology," IEEE Trans, Computer-Aided Design of integrated Circuits, vol. 16, pp. 1383-1389, Nov.1997.
- [12] I-Chyn Wey, Y-Gang Chen and An-Yeu Wu, "Design and analysis of Isolated Noise- Tolerant Technique in Dynamic CMOS Circuits," IEEE Trans.on VLSI sys. vol.16, no.12, pp. 1708-1712, Dec.2008
- [13] L. Wang and N. Shanbhag, "An energy-efficient noise-tolerant dynamic circuit design," IEEE Trans. Cir. & syst. II, vol. 47, pp. 1300-1306, Nov. 2000.
- [14] B.-Y. Tsui, L.-F. Chin, "A comprehensive study of the FIBL of nanoscale MOSFETs", IEEE Transactions on Electron Devices 51 (10) (2004) 1733–1735. [2] L. T. Clarke, G. F. Taylor, "High fan-in circuit design," IEEE Journal of Solid-State Circuits, vol. 31, Issue 1, January 1996, pp.91-96.
- [15] H. Mahmoodi and K. Roy, "Diode-footed domino: A leakage-tolerant high fan-in dynamic circuit design style," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 51, no. 3, pp. 495–503, Mar. 2004.
- [16] Preetisudha Meher, Kamalakanta Mahapatra "Modifications in CMOS Dynamic Logic Style: A Review Paper" J. Springer 2014.
- [17] R.H. Krambeck, C.M. Lee, H.F.S. Law, "High-speed compact circuits with CMOS" IEEE J. Solid-State Circuits SC-17, 614–619 (1982)
- [18] M.W. Allam, M.H. Anis, M.I. Elmasry, "High speed dynamic logic style for scaled down CMOS and MTCMOS technologies," in: Proceedings of the International Symposium on Low Power Electronics and Design, 2000, pp. 155–160.
- [19] Uday Panwar, Ajay Kumar Dadoria "Comparison on Different Domino Logic Design for High-performance and Leakage-Tolerant Wide OR Gate" ISSN : 2248-9622, Vol. 3, Issue 6, Nov-Dec 2013, pp.2048-2052.
- [20] Shiksha and Kamal Kant Kashyap "High Speed Domino Logic Circuit for Improved Performance" 978-1-4799-4939-7/14, 2014 IEEE.