



Design of High Speed Multiplier using Modified Carry Select Adder

Jasbir Kaur¹, Lalit Sood² and Neelam Rup Prakash³

Assistant Professor, ECE Department, PEC University of Technology, Chandigarh, India¹

PG Scholar, Electronics (VLSI Design), PEC University of Technology, Chandigarh, India²

Associate Professor, ECE Department, PEC University of Technology, Chandigarh, India³

Abstract: A system's performance is generally determined by the speed of the multiplier since multiplier is one of the key hardware components in high performance systems such as FIR filters, digital signal processors and microprocessors etc. Multipliers have large area, long latency and consume considerable power. Hence various multiplier architecture increases the efficiency and performance of a system. With the advances in technology, researchers have tried and are trying to design multipliers that offer either high speed, low power consumption, less area or the combination of these. In this paper, a 14-bit X 5-bit multiplier is designed using modified carry select adder which is efficient to increase the speed of multiplication. This modified carry select adder can add up to five 16-bit numbers. The design is simulated using Cadence Tool.

Keywords: Multiplier, Modified Carry Select Adder, High speed.

I. Introduction

The multipliers are the most important part of all digital signal processors; they are very important in realizing many important functions such as Fast Fourier Transforms and convolutions. Since a processor spends considerable amount of time in performing multiplication, an improvement in multiplication speed can greatly improve system performance. Multiplication can be implemented using many algorithms such as array, Wallace tree, carry save, and booth algorithms.

Multipliers require high amount of power and delay during the partial product addition. At this stage, most of the multipliers are designed with different kind of adders that are capable to add a number of bits using compressors at the cost of increased delay.

This paper proposes the design of high speed multiplier using modified carry select adder which has two main features. One is this multiplier involves the carry select addition that increases the speed of multiplication. Second is the compressors used for partial product addition operate simultaneously and are independent of previous stage outputs that also contribute in increasing the speed of multiplication. This paper is partitioned into six sections. Section II describes the conventional method for multiplication. Section III gives introduction to modified carry select adder. Section IV deals with design of modified carry select adder. Section V deals with the design of high speed multiplier. Section VI compares the results of designed multiplier with conventional one. Conclusions and references follow.

II. Conventional Multiplier

The basic algorithm for multiplication of two numbers, M (multiplier) and N (multiplicand), makes use of the distributive property of multiplication, i.e., if M can be written as sum of smaller numbers $M = M_0 + M_1 + \dots + M_{m-1}$, then the multiplication $M \cdot N$ can be written as

$$M \cdot N = (M_0 + M_1 + \dots + M_{m-1}) \cdot N \\ = M_0 \cdot N + M_1 \cdot N + \dots + M_{m-1} \cdot N \quad (1)$$

The terms on the right hand side are called partial products – smaller products, each one representing only a part of the total product. A multiplication algorithm finds a simple way to allow a simple calculation of the partial products. Then the total product is composed by summation of all partial products.

The value of a binary number $M = m_{m-1} \dots m_1 m_0$ can be written as

$$M = \sum_{i=0}^{m-1} m_i \cdot 2^i \quad (2)$$

Where m_i are the different bits of M , and m is the total number of bits.

If the partial products are $P_{m-1} \dots P_1 P_0$, then

$$P_0 = N \cdot m_0;$$

$$P_1 = N \cdot m_1; \text{ and embed one zero before least significant bit.}$$

...

$P_{m-2} = N \cdot m_{m-2}$; and embed $(m-2)$ zeros before least significant bit.

$P_{m-1} = N \cdot m_{m-1}$; and embed $(m-1)$ zeros before least significant bit.

Then, $M \cdot N = P_0 + P_1 + \dots + P_{m-2} + P_{m-1}$

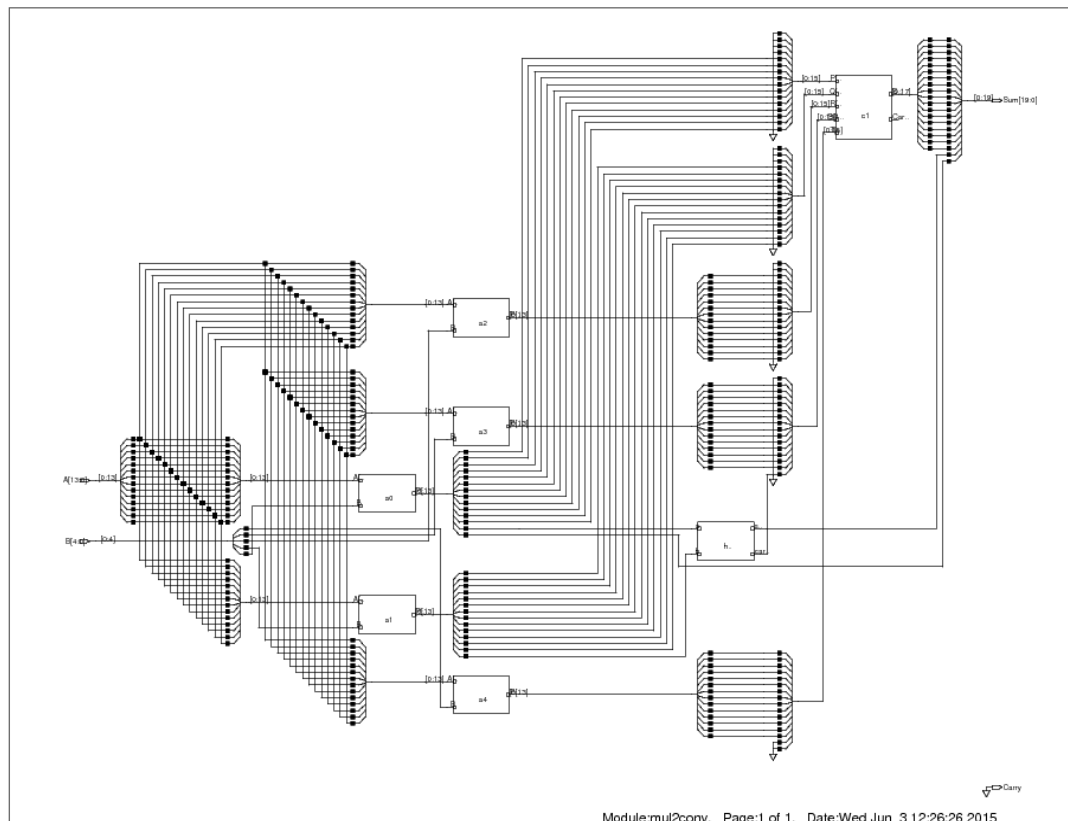
(3)

Special case: If $M = 5$ bit and $N = 14$ bit, then partial products are P_0, P_1, P_2, P_3 and P_4 .

A bit-wise addition of partial products for this special case using conventional method can be explained with the help of Table 1. The schematic diagram for the same is shown in Figure 1.

Table 1: Bit-wise addition of partial products using conventional method

Bits to be added	Sum	Carry [0]	Carry[1]
$P_0[0]$	$M.N[0]$	0	0
$P_0[1], P_1[1]$	$M.N[1]$	$C_1[0]$	0
$P_0[2], P_1[2], P_2[2], C_1[0]$	$M.N[2]$	$C_2[0]$	$C_2[1]$
$P_0[3], P_1[3], P_2[3], P_3[3], C_2[0]$	$M.N[3]$	$C_3[0]$	$C_3[1]$
$P_0[4], P_1[4], P_2[4], P_3[4], P_4[4], C_3[0], C_2[1]$	$M.N[4]$	$C_4[0]$	$C_4[1]$
$P_0[5], P_1[5], P_2[5], P_3[5], P_4[5], C_4[0], C_3[1]$	$M.N[5]$	$C_5[0]$	$C_5[1]$
$P_0[6], P_1[6], P_2[6], P_3[6], P_4[6], C_5[0], C_4[1]$	$M.N[6]$	$C_6[0]$	$C_6[1]$
$P_0[7], P_1[7], P_2[7], P_3[7], P_4[7], C_6[0], C_5[1]$	$M.N[7]$	$C_7[0]$	$C_7[1]$
$P_0[8], P_1[8], P_2[8], P_3[8], P_4[8], C_7[0], C_6[1]$	$M.N[8]$	$C_8[0]$	$C_8[1]$
$P_0[9], P_1[9], P_2[9], P_3[9], P_4[9], C_8[0], C_7[1]$	$M.N[9]$	$C_9[0]$	$C_9[1]$
$P_0[10], P_1[10], P_2[10], P_3[10], P_4[10], C_9[0], C_8[1]$	$M.N[10]$	$C_{10}[0]$	$C_{10}[1]$
$P_0[11], P_1[11], P_2[11], P_3[11], P_4[11], C_{10}[0], C_9[1]$	$M.N[11]$	$C_{11}[0]$	$C_{11}[1]$
$P_0[12], P_1[12], P_2[12], P_3[12], P_4[12], C_{11}[0], C_{10}[1]$	$M.N[12]$	$C_{12}[0]$	$C_{12}[1]$
$P_0[13], P_1[13], P_2[13], P_3[13], P_4[13], C_{12}[0], C_{11}[1]$	$M.N[13]$	$C_{13}[0]$	$C_{13}[1]$
$P_1[14], P_2[14], P_3[14], P_4[14], C_{13}[0], C_{12}[1]$	$M.N[14]$	$C_{14}[0]$	$C_{14}[1]$
$P_2[15], P_3[15], P_4[15], C_{14}[0], C_{13}[1]$	$M.N[15]$	$C_{15}[0]$	$C_{15}[1]$
$P_3[16], P_4[16], C_{15}[0], C_{14}[1]$	$M.N[16]$	$C_{16}[0]$	$C_{16}[1]$
$P_4[17], C_{16}[0], C_{15}[1]$	$M.N[17]$	$C_{17}[0]$	$C_{17}[1]$
$C_{17}[0], C_{16}[1]$	$M.N[18]$	$C_{18}[0]$	0
$C_{18}[0], C_{17}[1]$	$M.N[19]$	$C_{19}[0]$	0
$C_{19}[0]$	$M.N[20]$	0	0



Cadence Schematics, Copyright 1997-2006

Figure 1: Schematic diagram of conventional multiplier

III. Introduction to Modified Carry Select Adder (MCSIA)

Modified Carry Select Adder is designed to add up to five 16-bit numbers. This MCSIA is designed by using two components. First component is compressor that compresses five bits into two bits. Second component is carry select adder that generates the result by using ripple carry adders and multiplexers.

A. Compressor

For compressing five bits into two bits, two compressors are used. One is 5:3 compressor and another one is 3:2 compressor.

(i) 5:3 Compressor

5:3 Compressor is made up of two full adders and one half adder. It is designed to add five bits and generates final sum of three bits [6, 7]. The block diagram of 5:3 compressor is shown in Figure 2(a).

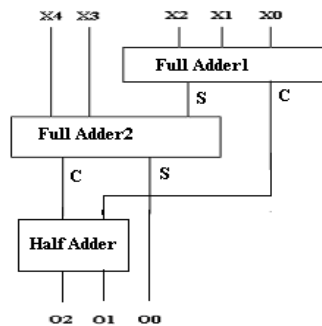


Figure 2(a): Block Diagram of 5:3 Compressor

(ii) 3:2 Compressor

3:2 Compressor is simply a full adder that adds three bits and generates two bit output as sum and carry. The block diagram of 3:2 compressor is shown in Figure 2(b).

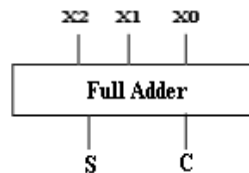


Figure 2(b): Block Diagram of 3:2 Compressor

B. Carry Select Adder (CSIA)

Carry Select Adder architecture consists of independent generation of sum and carry i.e., $C_{in}=1$ and $C_{in}=0$ are executed in parallel [5]. Depending upon C_{in} , the external multiplexers select the carry to be propagated to next stage. Further, based on the carry input, the pre calculated sum is selected and delay is reduced. However, the structure is increased due to the complexity of multiplexers [3]. The architecture of CSIA is shown in Figure 3.

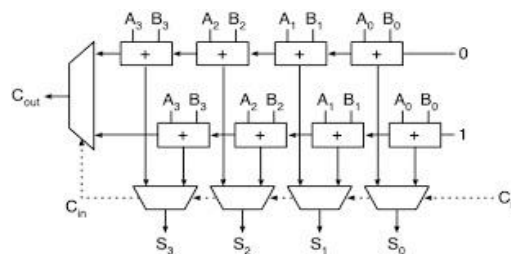


Figure 3: Block Diagram of CSIA

IV. Design of Modified Carry Select Adder

This Modified Carry Select Adder takes five 16-bit numbers P, Q, R, S and T as input and generates 18-bit sum and a carry. The architecture of MCSIA is described step by step with the help of Figure 4(a), Figure 4(b), Figure 4(c), Figure 4(d) and Figure 4(e). The schematic diagram for MCSIA is shown in Figure 5.

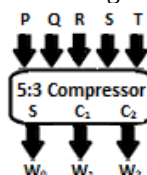


Figure 4(a): 16-bit 5:3 Compressor

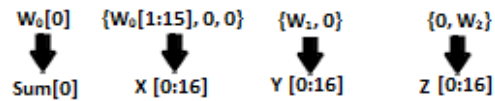


Figure 4(b): Rearrangement of bits

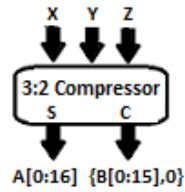


Figure 4(c): 17-bit 3:2 Compressor

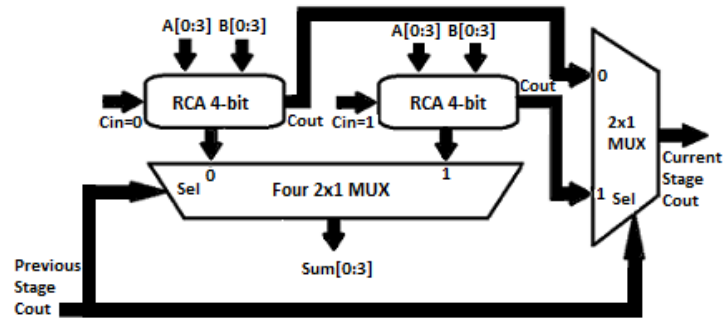


Figure 4(d): Basic Block of CS/A

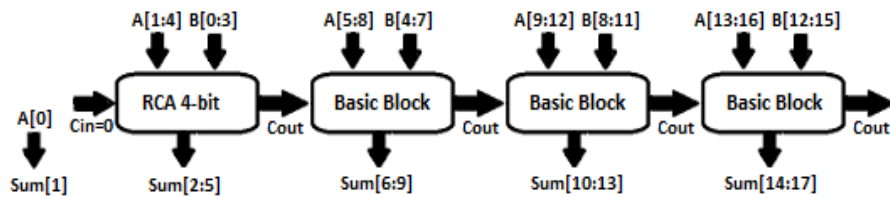
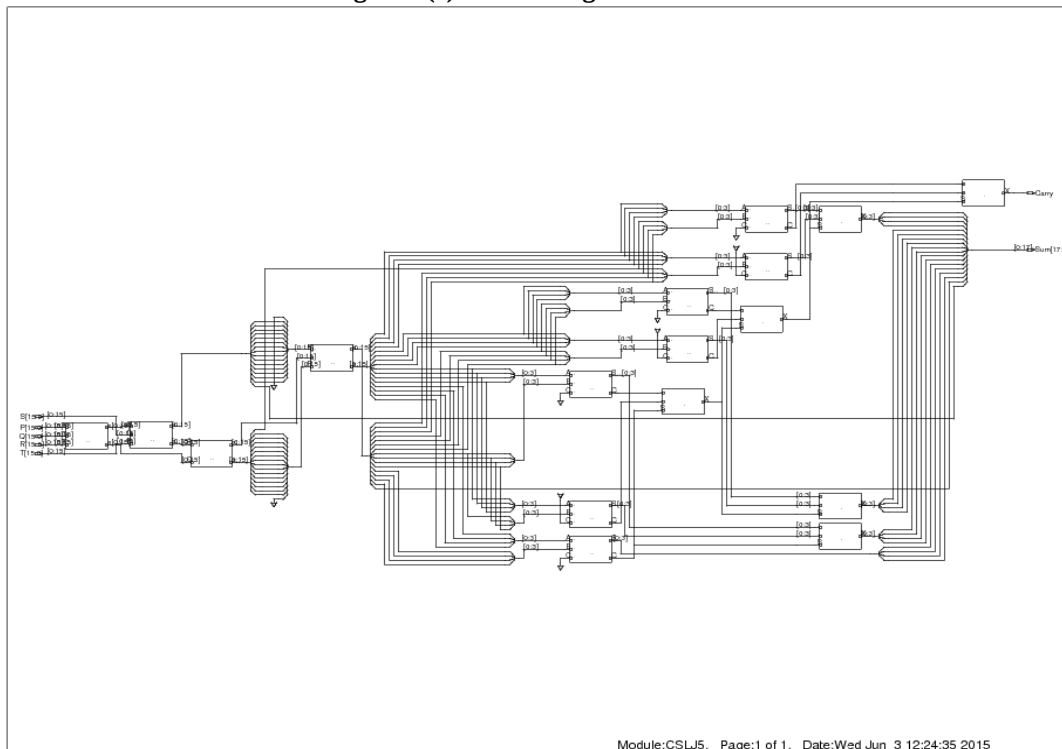


Figure 4(e): Block Diagram of CS/A



Module:CS/A, Page:1 of 1, Date:Wed Jun 3 12:24:35 2015

Cadence Schematics, Copyright 1997-2006

Figure 5: Schematic diagram of MCS/A

V. Design of High Speed Multiplier using Carry Select Adder

The designed high speed multiplier can be divided into two parts- partial product generator and modified carry select adder. The partial product generator involves the logical AND operation and bit shifting. The modified carry select adder generates the result by adding partial product terms.

A. Partial Product Generator

It generates partial product terms $P_0P_1P_2P_3P_4$ by using 5-bit multiplier M and 14-bit multiplicand N as per following equations:

$$P_0 = N \text{ AND } M[0];$$

$$P_1 = N \text{ AND } M[1]; \text{ and embed one zero before least significant bit.}$$

$$P_2 = N \text{ AND } M[2]; \text{ and embed two zeros before least significant bit.}$$

$$P_3 = N \text{ AND } M[3]; \text{ and embed three zeros before least significant bit.}$$

$$P_4 = N \text{ AND } M[4]; \text{ and embed four zeros before least significant bit.}$$

B. Modified Carry Select Adder

Modified carry select adder takes P_0, P_1, P_2, P_3 and P_4 as input and generates the result $M.N$.

The block diagram of designed high speed multiplier using a half adder and modified carry select adder is shown in Figure 6. The schematic diagram for high speed multiplier using MCSIA is shown in Figure 7.

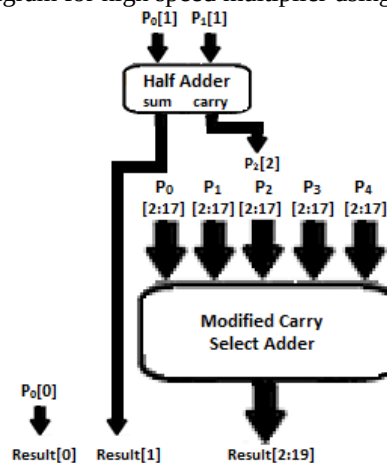
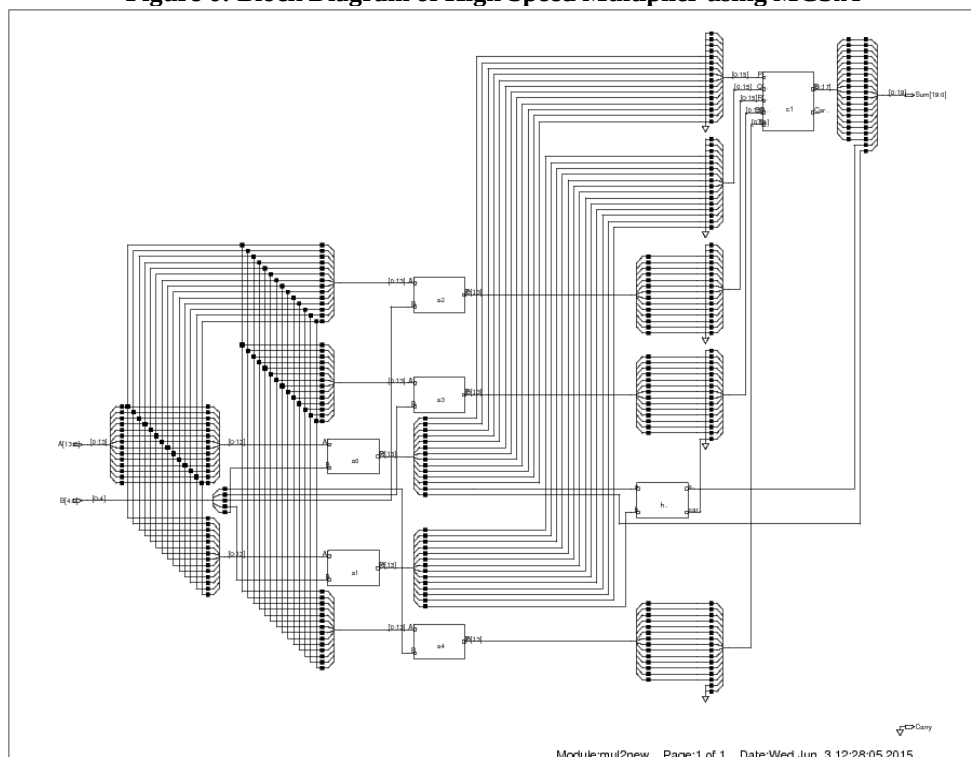


Figure 6: Block Diagram of High Speed Multiplier using MCSIA



Cadence Schematics, Copyright 1997-2006

Figure 7: Schematic diagram of high speed multiplier using MCSIA

VI. Comparison

In this paper the proposed high speed multiplier using modified carry select adder and conventional multiplier have been simulated using Cadence Tool. The comparison is done on the basis of parameters- power consumption, speed of operation and area used. The comparative results of these two multipliers are shown in Table 2.

Table 2: Comparison between proposed multiplier and conventional multiplier

Parameter	% increase/decrease for proposed multiplier as compared to conventional multiplier
Power	48.22 % increased
Delay	80.27 % decreased
Area	30.20 % increased

VII. Conclusions

Different types of adder topologies are used to add the partial products [1]. On comparing different adder topologies, it is found that carry select adder is the fastest one among other mostly used adders [2]. The carry select adder is modified to add up to five 16-bit and used it for the addition of partial products generated during multiplication. This designed multiplier is 80.27% faster than conventional multiplier. It can be used for high speed applications where area and power consumption are not major issues.

VIII. References

- [1] R.Uma, Vidya Vijayan, M. Mohanapriya, and Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies", International Journal of VLSI Design & Communication Systems, vol.3, no.1, pp.153-168, Feb 2012.
- [2] Jasbir Kaur, Lalit Sood, "Comparison Between Various Types of Adder Topologies", IJCST vol.6, Issue 1, Jan-March 2015.
- [3] Sarabdeep Singh, Dilip Kumar, "Design of Area and Power Efficient Modified Carry Select Adder", International Journal of Computer Applications, vol.33, no.3, pp.14-18, Nov 2011.
- [4] Padma Devi, Ashima Girdher and Balwinder Singh, "Improved Carry Select Adder with Reduced Area and Low Power Consumption", International Journal of Computer Application, Vol 3.No.4, June 2010 .
- [5] Romana Yousuf and Najeeb-ud-din, "Synthesis of Carry Select Adder in 65 nm FPGA", IEEE.
- [6] J. Gu, C. Chang (2003), "Ultra low voltage low power 4-2 compressor for high speed multiplications", Proceedings of IEEE International Symposium on Circuits and Systems", Vol. 5, pp. 321-324.
- [7] K. Prasad, K.K. Parhi (2001), "Low power 4-2 and 5-2 compressors", Proceedings of 35th Asilomar Conference on Signals, Systems and Computers, Vol. 1, pp. 129-133.
- [8] V.G. Oklobdzija, D. Villeger, S.S. Liu (1996), "A method for speed optimized partial product reduction and generation of fast parallel multipliers using an algorithmic approach", IEEE Transactions on Computers, Vol. 45, No. 3.
- [9] P. Stelling, C. Martel, V.G. Oklobdzija, R. Ravi (1998), "Optimal circuit for parallel multipliers", IEEE Transactions on Computers, Vol. 47, No. 3.
- [10] V.G. Oklobdzija (2000), "High speed VLSI arithmetic unit: Adders and Multipliers", in Design of High Performance Microprocessor Circuits", Editor A. Chandrakasan, IEEE Press.