



A Review and comprehensive study of 6-bit Flash Analog to Digital Converter

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Abstract: Power consumption has become a main problem in VLSI especially the static power consumption. So to reduce this in 6-bit flash ADC, we have reduced the number of components in the circuit. This reduction is accomplished using multiplexing technique. The technique reduces the number of comparators and pre-amplifiers. A simple N-bit flash ADC requires $2N-1$ preamplifiers and comparators while this design requires only $2^{(N-3)} + 2$ preamplifiers and $2^{(N-2)} + 1$ comparators. Also distortion at higher frequencies is reduced in the design.

Keywords: Flash ADC, Multiplexer, pre-amplifiers, resistance ladder, thermometer to binary encoder, interpolated comparator.

I. Introduction

In this era of electronic gadgets, mobile and communication based systems mainly require ADC circuit at initial stages. The ADC used in devices must operate at lower power source with minimum delays and lower power dissipation. However, the large number of preamplifiers and comparators connected to input results in a voltage variable junction capacitance. This signal dependency of capacitance leads to lower effective number of bit (ENOB) and higher distortion at increasing input frequencies. The modified design has smaller size and lower power dissipation. Further, the operating speed can be improved because the total input capacitance of the preamplifiers and comparators can be reduced substantially.

II. Design and Operation

The modified design comprises of following components:

- A resistive reference ladder
- A passive Track and Hold circuit
- A 2:1 and eight 4:1 multiplexer
- 10 pre amplifier
- 17 comparators
- A 4-bit thermometer to binary encoder

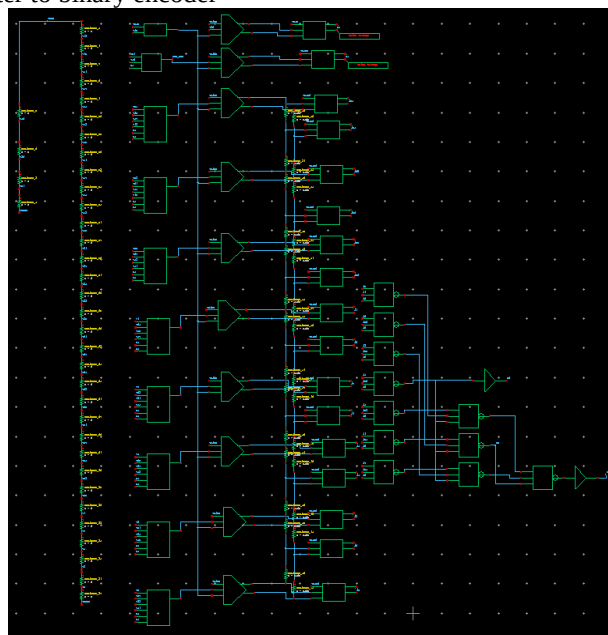


Fig.1 ADC

III. Working

Resistance Ladder

The ladder is provided in the circuit to get different voltage levels so that they can be compared with the input signal which correspondingly turns the comparator ON or OFF. With the Help of reference ladder we have generate 16 different Voltage levels. Further another ladder is used to select different states of multiplexer.

Track and Hold Circuit

This circuit is used to hold the input signal data at the clock so that it can be easily compared with the different voltage levels. A differential bootstrap circuit is needed with a pulsed output voltage greater than $V_{DD} + V_{THN}$ to fully turn on the sampling switch. It can reduce the signal dependence and the second order distortion at the time of sampling.

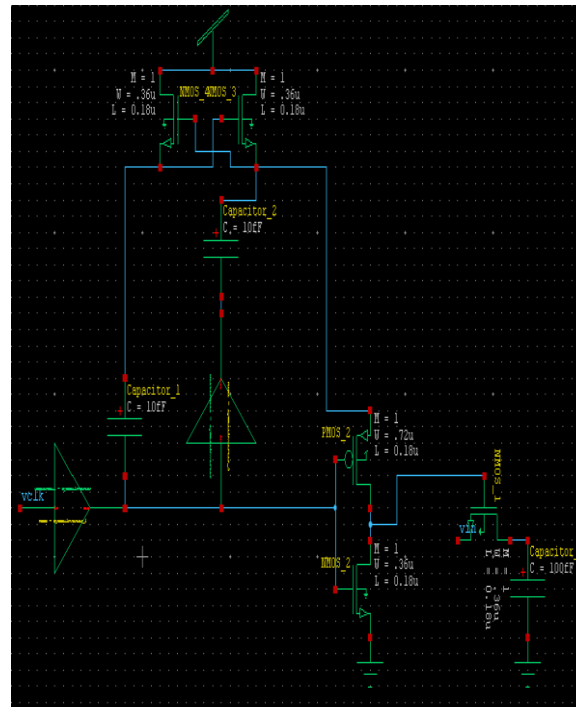


Fig.2 Track and hold circuit

Pre-amplifier

This circuit amplifies the differential voltage obtained from the Track & Hold circuit and the reference voltages. The preamplifier amplifies the input signal to enhance the comparator sensitivity and isolates the input of the comparator from switching noise present in the circuit.

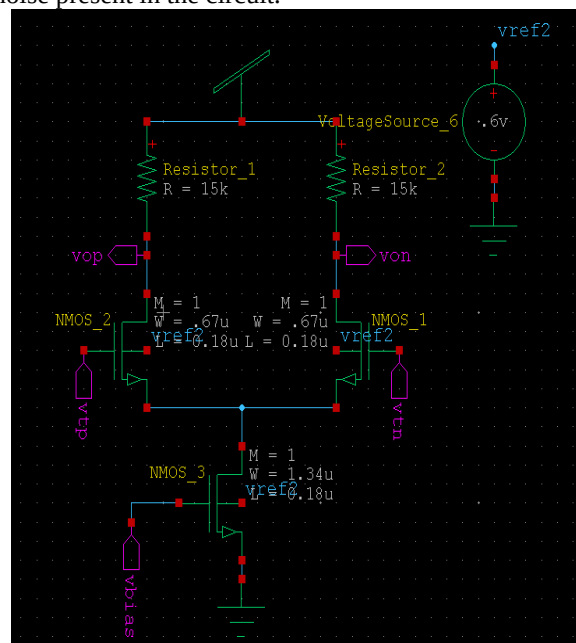


Fig.3 Pre amplifier

Multiplexer

The number of comparators and pre amplifier are reduced due to multiplexer. The multiplexer selects the different voltage levels according to the select lines. The multiplexer is employed so that same comparators and pre-amplifiers can be used again in circuitry for different voltage levels comparisons. This can be easily seen by analyzing the schematic design.

Comparators

It is used to compare the input signal with the reference voltage levels. The cross-coupled inverter placed above the input pair regenerates the input analog signal into a full-scale digital signal. This circuit is connected with SR latch to hold the output from the comparator. This gives the output at clock pulse when the input is greater than the reference voltage level. The circuit is shown in the figure described below.

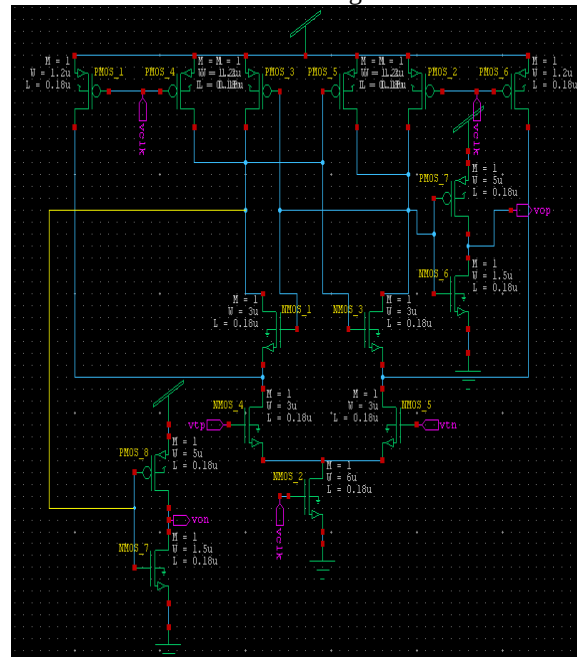


Fig.4 Comparator

Thermometer-to-binary encoder

It is used to encode the output of interpolated comparator. The output from comparators is in form of thermometer code. This is the multiplexer based encoder circuit and there is lower problem of bubble error in this encoder and requires less hardware. Also there is a shorter critical path, which makes it useful for circuits with lower power consumption.

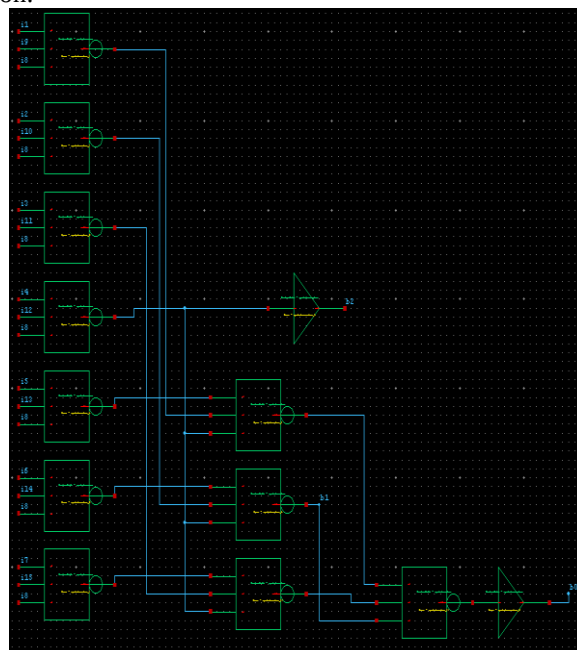


Fig.5 Encoder

IV. Conclusion

The circuit design is very efficient in terms of response time and power consumption. Due to decreased circuitry, it can operate at higher frequencies of up to 500 MHz without degradation of parameters like ENOB, SFRD, SNDR and Figure of Merit.

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