



## TBSC Compensator: Application and Simulation Results for Starting and Voltage Sag Mitigation of Induction Motor

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**Abstract:** This dissertations work deals with the analysis, design and implementation of Thyristor Binary Switched Capacitor (TBSC) banks. The performance of various TBSC topologies for reactive power compensation suitable for fast dynamic loads in closed loop systems are investigated by simulation. The scheme consists of Thyristor Binary Switched Capacitor (TBSC) banks. TBSC is based on a chain of Thyristor Switched Capacitor (TSC) banks arranged in binary sequential manner. Frequent switching of capacitors reduces the life of switched capacitor bank. Hence, a control circuitry has been proposed in such a way that transient free switching of TBSCs will takes place. Proposed topology allows almost step-less reactive power compensation for fast varying dynamic loads in closed loop. This scheme has error in reactive power compensation equals to half of the lowest step size of the capacitor bank. The suitable chain of binary switched capacitor bank will be proposed. The proposed scheme can achieve reactive power compensation cycle to cycle basis and the harmonics contents of sours are maintained at insignificant levels due to filtering action of TBSC as well as transient free switching of capacitor bank.

Proposed TBSC scheme compensates the fast varying dynamic reactive load. Also the proposed scheme can be used for direct online starting of I.M.s with voltage sag mitigation at starting, which helps improving stability of the system and Power Factor (P.F.) improvement in steady state.

**Keywords:** Reactive power compensation, TBSC, transient free switching, voltage sag, power factor, dynamic load, starting of induction motor.

### I. Introduction

It is well documented in literature and through public discussions at various levels that a substantial power loss is taking place in our low voltage distribution systems on account of poor power factor, due to inadequate reactive power compensation facilities and their improper control. Switched LT capacitors can directly supply the reactive power of loads and improve the operating condition. Government of India has been insisting on shunt capacitor installations in massive way and encouraging the state electricity boards through Rural Electrification Corporation and various other financing bodies. The expansion of rural power distribution systems with new connections and catering to agricultural sector in wide spread remote areas, giving rise to more inductive loads resulting in very low power factors [1].

The voltages at the remote ends are low and the farmer's use high HP motors operating at low load levels with low efficiencies. This is giving rise to large losses in the distribution network. Thus there exists a great necessity to closely match reactive power with the load so as to improve power factor, boost the voltage and reduce the losses. The conventional methods of reactive power supply are through switched LT capacitors, mostly in equal steps in various automatic power factor controllers developed by number of companies. In this paper, a more reliable, technically sound, fast acting and low cost scheme is presented by arranging the thyristor switched capacitor units in five binary sequential steps. This enables the reactive power variation with the least possible resolution. As there is reduction in loss with shunt compensation in the feeders, the efficiency increases and conservation of energy takes place. Besides the enhancement of transformer loading capability the shunt capacitor also improves the feeder performance, reduces voltage drop in the feeder and transformer, better voltage at load end, improves power factor and improves system security, increases over all efficiency, saves energy due to reduced system losses, avoids low power factor penalty, and reduces maximum demand charges [2&3].

Induction motors (I.M.) load constitute a large portion of power system. Three-phase induction motors represent the most significant load in the industrial plants, over the half of the delivered electrical energy. Starting of induction motor may cause a problem of voltage sag in the power system. The IEEE defines voltage sag as: A

decrease to between 0.1 and 0.9 p.u. in rms voltage or current at the power frequency for durations of 0.5 cycle to 1 min. An induction motor at rest can be modeled as a transformer with the secondary winding short circuited. Thus when full voltage is applied, a heavy inrush current (of 6 to 10 times the rated value) is drawn from the power system that causes voltage sag. As the motor accelerates and attains the rated speed, the inrush current decays and the system voltage recovers [4].

Voltage sag can cause mal-operation of voltage sensitive devices such as computers, relays, programmable logic controllers etc. Also because of the highly inductive nature of the motor circuit at rest, the power factor is very low, usually of the order of 10 to 20 percent. Thus reactive power demand at the starting of I.M. is very high and it reduces as motor picks up the speed. There are several solutions to minimize this problem; the most common are reactor start, auto transformer start, star-delta, capacitor start, soft starter, frequency variable driver (FVD) etc. All these methods except capacitor start are based on a motor terminal voltage reduction to decrease the rotor current, reducing the line voltage drop. Problem with this method of starting is that the motor torque is directly proportional to the square of the supply voltage hence decrease in the motor terminal voltage will cause the motor torque to decrease, which may be insufficient for driving the required load. Soft starter and frequency variable driver methods are the most expensive and complex, requiring more expert maintenance. In capacitor start system, reactive current required by the motor during acceleration is supplied by capacitors which reduce the source current. This in turn reduces the magnitude of voltage sag in the system. Capacitor start method has a lower cost in comparison with other methods however one has to consider the transitory effects of switching of capacitor banks [5&6].

The desirable features of the proposed scheme are as follows [7&8]:

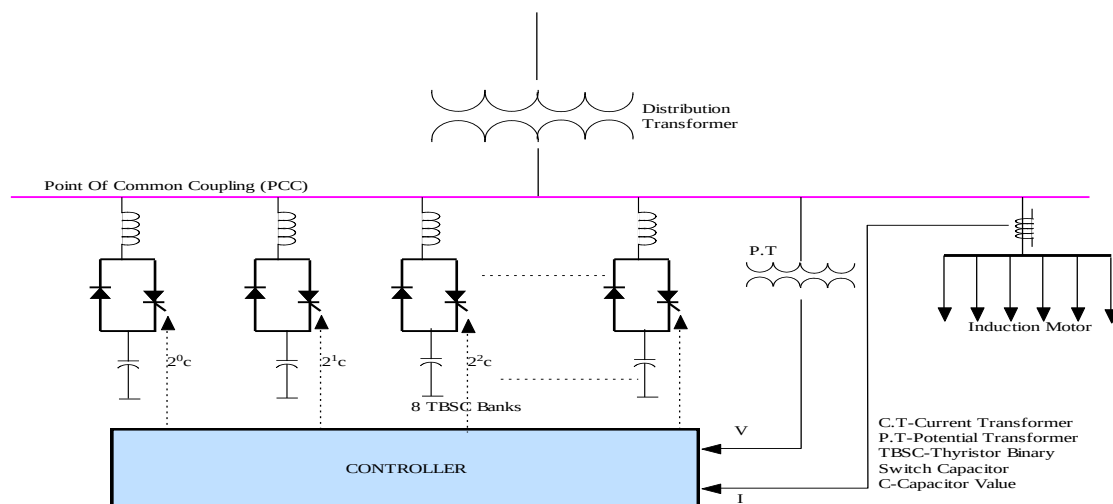
- It maintains the power factor at the PCC to any specified value.
- It compensates for rapid variation in reactive power or voltages.
- Maximum compensation time is 20 msec.
- No transients or harmonics are allowed to be present due to fast selective instants of switching in well co-ordinate manner.
- It is adaptive in the sense that the amount of the compensation is determined and provided on a cycle by cycle basis.
- It can compensate each phase independently which makes ideal for unbalanced systems.
- Capacitors are sized in binary sequential ratio for minimum size of switching steps.
- The control strategy is error activated to match with the load reactive power for the chosen time interval.
- It eliminates possible over compensation and resulting leading power factor.
- It is flexible to choose required number of steps as per the resolution.
- Resolution can be made small with more number of steps.
- Simple in principle, elegant in usage and of low cost

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## II PROPOSED TOPOLOGY

Following figure shows the schematic block diagram of proposed work.

**Figure.1. TBSC Compensator**



This paper presents a topology, which is shown in Fig.1. The proposed scheme consists of Thyristor Switched Capacitor (TSC) banks in binary sequential steps known as Thyristor Binary Switched Capacitor (TBSC) [9&10]. This TBSC facilitates step-less control of reactive power closely matching with load requirements so as to maintain desired power factor. The proposed topology has following distinctive features [2]:

- TSC (Thyristor Switched Capacitor) banks are arranged in Binary sequential steps to provide almost continuous reactive power compensation.
- Transient free switching is obtained by switching the capacitors to the negative/positive peak of supply voltage and firing the thyristors at the negative/positive peak of supply voltage.
- It compensates for rapid variation in reactive power.
- Reactive power compensation is achieved in cycle by cycle basis. That is step-less compensation.
- Inrush current problems during connection and Outrush current disconnection are avoided.

At the distribution transformer requiring total reactive power  $Q$  for improving the power factor from some initial value  $P.f1$  to the desired value  $P.f2$  at the load. This  $Q$  can be arranged in binary sequential 'n' steps, satisfying the following equation [1]:

$$Q = 2^n C + 2^{n-1} C + \dots + 2^2 C + 2^1 C + 2^0 C$$

The schematic diagram of the capacitor bank in five binary sequential steps through thyristor and with respective current limiting reactors is shown in Fig.1. TBSC compensator connected at the point of common coupling (PCC) for reactive power compensation is shown in Fig.1 and the operating principle of each equipment is analyzed in the following sections.

#### A TBSC:

TBSC consists of an anti-parallel connected thyristor as a bidirectional switch in series with a capacitor and a current limiting small reactor. Transient free switching of capacitors is obtained by satisfying following two conditions

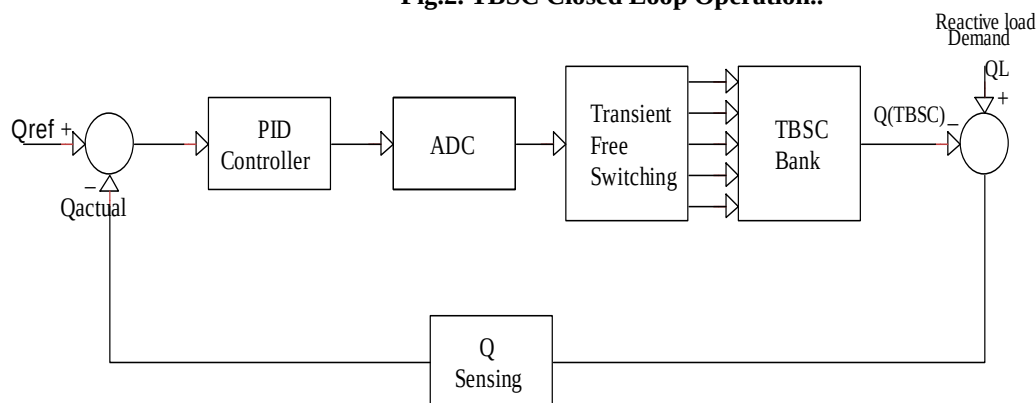
- Firing the thyristors at the negative/positive peak of supply voltage.
- Pre-charging the Capacitors to the negative/positive peak of supply voltage.
- TBSC current is sinusoidal and free from harmonics, thus eliminating the need for any filters. Small-series inductor is placed in series with capacitor. It serves following purposes:
- It limits current transients during overvoltage conditions and when switching at incorrect instants or at the inappropriate voltage polarity.
- The chosen inductor magnitude gives a natural resonant frequency of many times the system nominal frequency. This ensures that the inductance neither creates a harmonic-resonant circuit with the network nor dampers the TBSC control system.

In the proposed scheme, capacitor bank step values are chosen in binary sequence weights to make the resolution small. If such 'n' capacitor steps are used then  $2n$  different compensation levels can be provided [4]. In this scheme five TBSC banks are arranged as 2.5, 5, 10, 20, 40 KVAR in star connected with neutral grounded configuration.

#### B TBSC Closed Loop Operation:

A block diagram of reactive power compensator using TBSC banks is shown in Fig.2. Reference reactive power,  $Q_{ref}$  is calculated from the desired power factor. Actual reactive power at PCC,  $Q_{actual}$  is calculated by sensing voltage and current at PCC by P.T. and C.T. respectively. Error between  $Q_{ref}$  and  $Q_{actual}$  is given to PI Controller. A Discrete PI Controller is used. Output of PI Controller is given to ADC and its output is given to TBSC banks in such a way that no transients occur. In this way closed loop operation of TBSC banks for reactive power compensation is achieved. [12]

Fig.2. TBSC Closed Loop Operation..

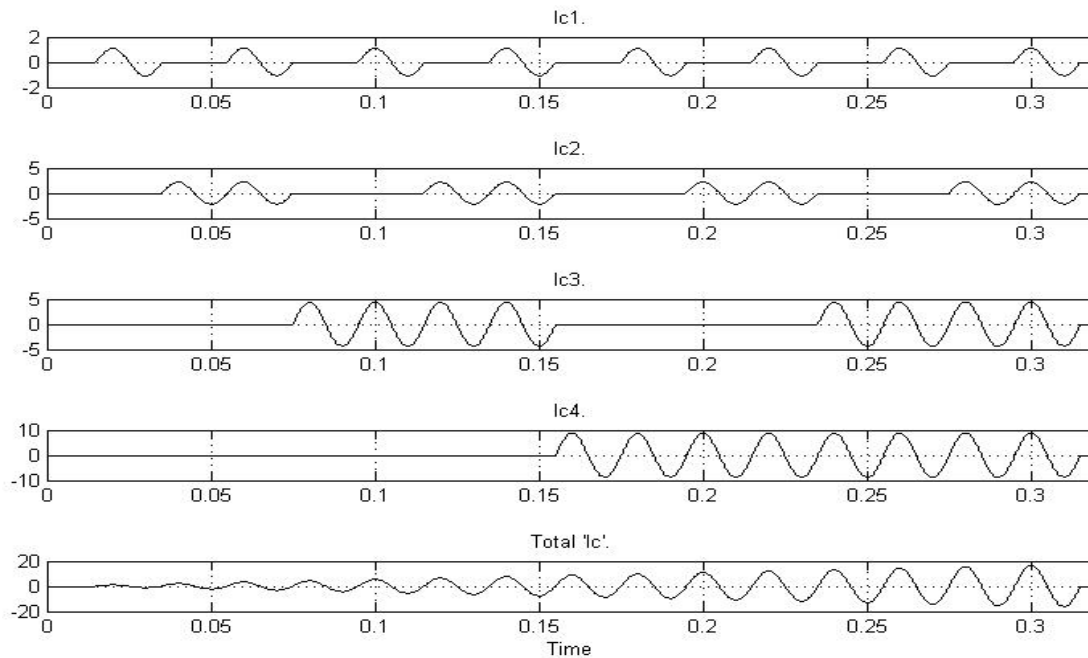


### III MATLAB SIMULATION RESULTS

#### A. Binary Current and Voltage Generation:

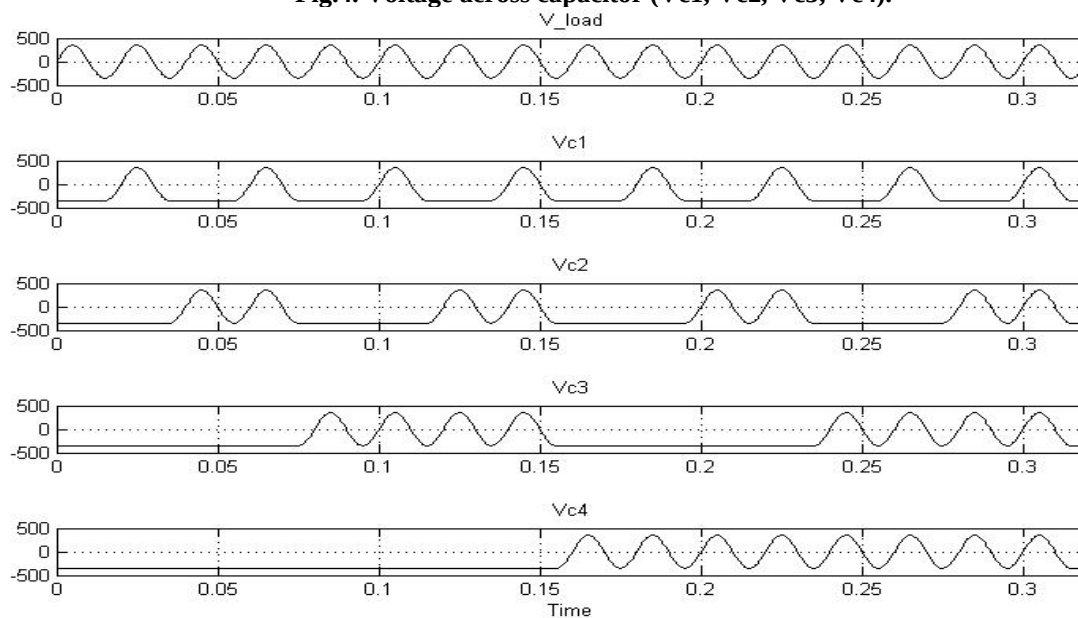
The Fig.3 shows the binary operation of the TBSC compensator proposed in fig.1. The total compensating current from phase "R" (total  $i_c$ ), is being increased step by step. The capacitor currents from the branches B1 ( $i_{c1}$ ), B2 ( $i_{c2}$ ), B4 ( $i_{c4}$ ), and B8 ( $i_{c8}$ ) are shown in fig.3 respectively. In fig.3 the total compensating current for the phase "R" (total  $i_c$ ) is displayed ( $\text{total } i_c = i_{c1} + i_{c2} + i_{c4} + i_{c8}$ ). [11]

**Fig.3. Compensating current for phase "R".**  
( $i_{c1}$ ) Current through B1      ( $i_{c2}$ ) Current through B2  
( $i_{c3}$ ) Current through B4      ( $i_{c4}$ ) Current through B8



It can be noted that harmonics or inrush problems are not generated, and that the current total  $i_c$  seems to vary continuously. The transitions during connection and disconnection are quite clean.

**Fig.4. Voltage across capacitor ( $V_{c1}$ ,  $V_{c2}$ ,  $V_{c3}$ ,  $V_{c4}$ ).**



### B. TBSC Compensator for fast varying dynamic load:

Data used in Simulation:-

Source Voltage,  $V = 400$  V,  $R_s = 0.0287\Omega$ ,  $L_s = 0.20471$ mH.

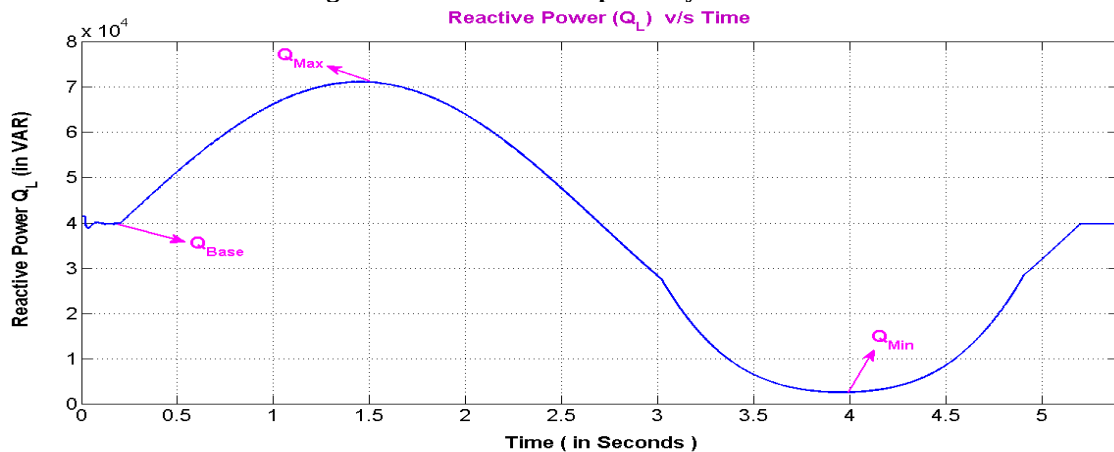
TBSC banks:- Five TBSC banks are used in the simulation whose values are shown in Table I. Continuously changing reactive power,  $Q_L$  is obtained by simulating three phase dynamic load. The nature of load variation is as shown in Fig.4.

**Table I:** Values of five TBSC banks

| Sr. No. | Q in KVAR | C in $\mu$ f | L in mH |
|---------|-----------|--------------|---------|
| 1.      | 2.5       | 45           | 0.32    |
| 2.      | 5         | 90           | 0.16    |
| 3.      | 10        | 180          | 0.08    |
| 4.      | 20        | 360          | 0.04    |
| 5.      | 40        | 720          | 0.02    |

Minimum reactive power  $Q_{min}$ , maximum reactive power  $Q_{max}$ , and base reactive power  $Q_{base}$  can be varied by changing the parameters of three phase dynamic.

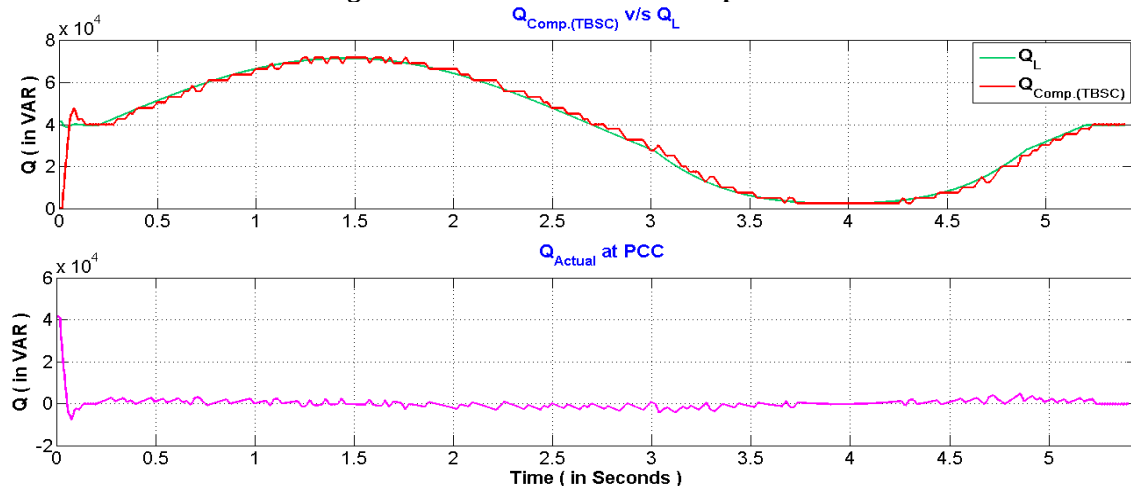
**Fig.4. Simulation of three phase dynamic load.**



### C. TBSC Closed Loop Operation for dynamic load:

Discrete PI controller with  $K_P = 0.565$  and  $K_I = 25$  is used. 5 bit ADC is used in simulation. Parameters of Three-phase dynamic load block are adjusted in such a way that  $Q_L$  varies continuously from  $Q_{min} = 0.25$  KVAR to  $Q_{max} = 77.5$  KVAR with base load  $Q_{base} = 40$  KVAR. This variation takes place in five seconds. Waveforms of load reactive power  $Q_L$ , reactive power given by TBSC,  $Q_{comp.}(TBSC)$  and actual reactive power  $Q_{Actual}$  at PCC are shown in Fig.5.

**Fig.4. Simulation Result of TBSC operation.**



From simulation results it is seen that  $Q_{comp.}(TBSC)$  closely follows  $Q_L$  shown in Fig.4, and actual reactive power  $Q_{Actual}$  at PCC is approximately +500 to -500 VARs at all discrete switching instances. The small error is due to the binary switching arrangement of TBSCs. These errors can be minimized by adding more number of capacitor banks in TBSC.

**Fig.5. Current waveforms through all TBSC bank and source (of R phase only).**

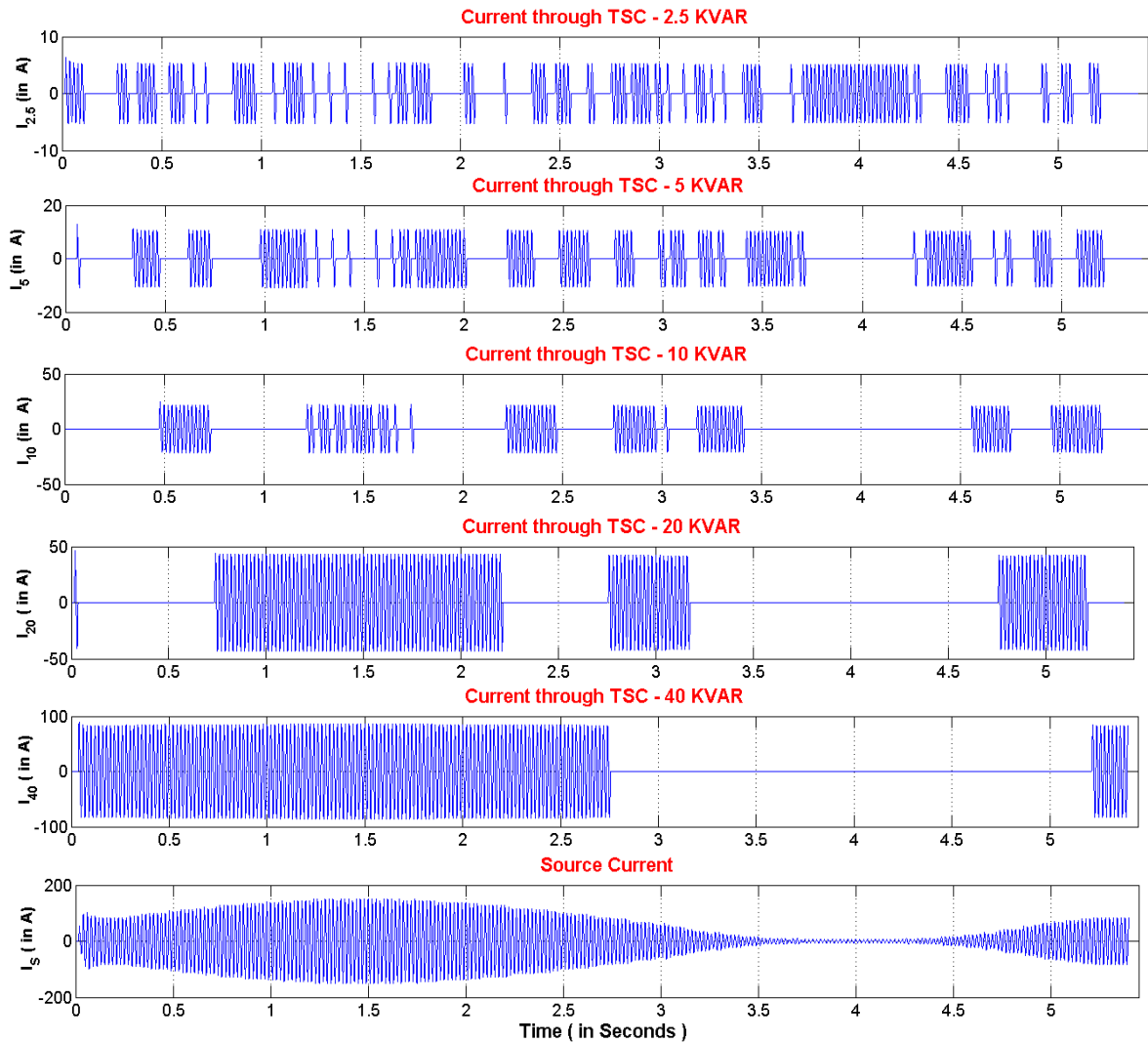


Fig.5 clearly shows the current waveforms which are free from both harmonics and transients.

#### **D. TBSC Compensator for voltage sag mitigation of induction motors:**

Data used in the simulation is shown below.

- Source Voltage,  $V = 400$  V,  $R_s = 0.0287\Omega$ ,  $L_s = 0.20471$  mH
- Induction motor (I.M.) – Three identical I.M.s are used in the simulation which are switched on at  $t = 0$  sec, 0.8 sec and 1.6 sec respectively. For Simulation purpose at 1.6 sec, two 50 h.p. motors are switched on simultaneously to get 100 h.p. load

**Table III:**

| Sr. No. | Parameter     | Value   |
|---------|---------------|---------|
| 1.      | Line Voltage  | 400v    |
| 2.      | Frequency     | 50H.z   |
| 3.      | Nominal Power | 50HP    |
| 4.      | Speed         | 1440rpm |

**Table IIIII: Values of Eight TBSC banks are shown in**

| Sr. No. | Q(in KVAR) | C (in $\mu$ F) | L (in mH) |
|---------|------------|----------------|-----------|
| 1.      | 2.5        | 50             | 0.10775   |
| 2.      | 5          | 100            | 0.0538    |
| 3.      | 10         | 200            | 0.0269    |
| 4.      | 20         | 400            | 0.0134    |
| 5.      | 40         | 800            | 0.0067    |
| 6.      | 80         | 1600           | 0.0033    |
| 7.      | 160        | 3200           | 0.0016    |
| 8.      | 320        | 6400           | 0.00084   |

Fig.6. shows the waveform of motor line voltage. When I.M.1 is switched on at  $t=0$ sec, the motor line voltage drops to 351V i.e. voltage sag of 11.14% takes place. Line voltage returns to steady value of 395V in 0.5sec. When I.M.2 is switched on at  $t=0.8$ sec, the motor line voltage drops to 349V i.e. voltage sag of 11.64% takes place. Line voltage returns to steady value of 392V in 0.5sec. When I.M.3 is switched on at  $t=1.6$ sec, the motor line voltage drops to 309V i.e. voltage sag of 21.77% takes place. Line voltage returns to steady value of 382V in 0.7sec

**Fig.6. Motor Line Voltage without TBSC compensator**

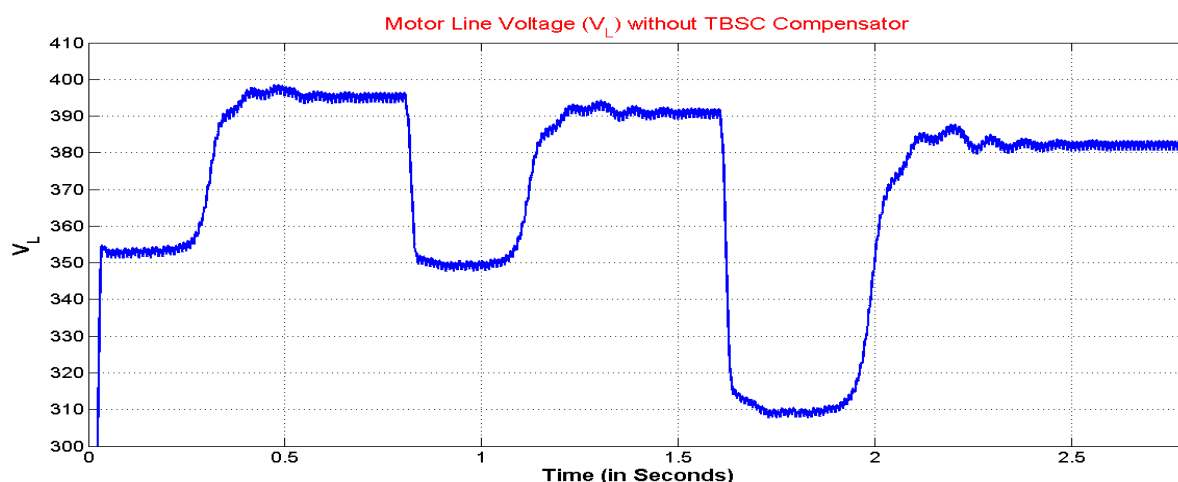


Fig.7. shows the variation of reactive power with time. When I.M.1 & 2 is switched on at  $t= 0$ sec and 0.8sec respectively, reactive power demand is around 250 KVAR at starting period. Reactive power demand is around 380 KVAR when I.M.3 is switched on at  $t=1.6$  sec. It is seen that reactive power demand is very high at the time of starting of motor and it reduces as the motor reaches the steady state condition. Because of high reactive power requirement at start voltage drops as shown in Fig. 6.

**Fig.7. Reactive Power variation of I.M. without TBSC compensator**

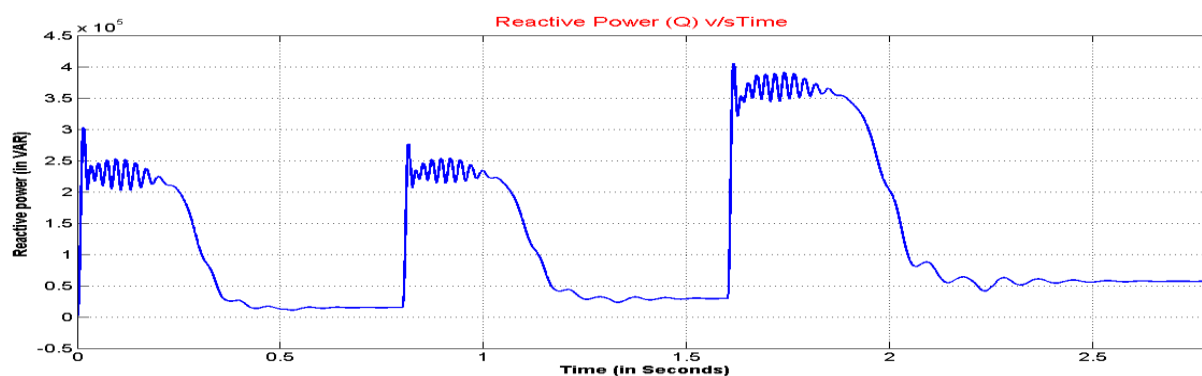


**Fig.8. Motor line current without TBSC compensator.**

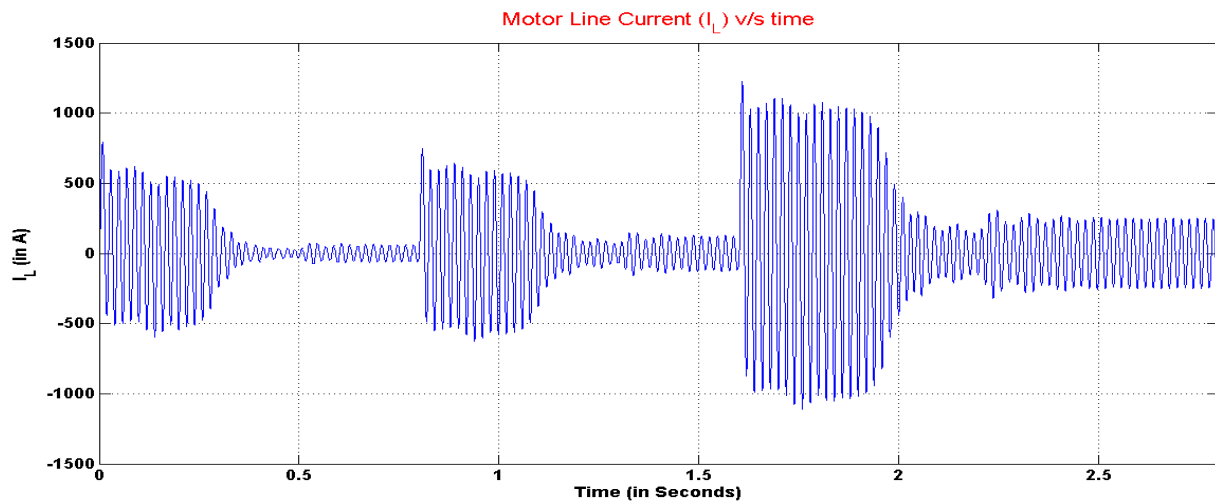


Fig.8 shows the variation of motor current with time. When I.M.1 & 2 is switched on at  $t = 0$ sec and 0.8 sec respectively, current is around 500 A at starting period while at the time of starting of I.M. 3 it is around 1000 A. It is seen that when motor is switched on, current is very large at the starting period & it reduces as motor attains steady speed.

#### **E. TBSC Closed Loop Operation for Induction Motor load:**

Discrete PI controller with  $K_P = 0.54$  &  $K_I = 25$  is used. 8 bit ADC is used in simulation. Waveforms of I.M. reactive power demand  $Q_{Motor}$  and reactive power given by TBSC  $Q_{TBSC}$  are shown in Fig. 9. From simulation results it is seen that  $Q_{TBSC}$  closely follows  $Q_{Motor}$  and actual reactive power  $Q_{Actual}$  at PCC is approximately zero at all times. Thus power factor is maintained near unity at all time. The small error is due to the binary switching arrangement of TSCs

**Fig.9. Waveforms of  $Q_{Motor}$  and  $Q_{TBSC}$**

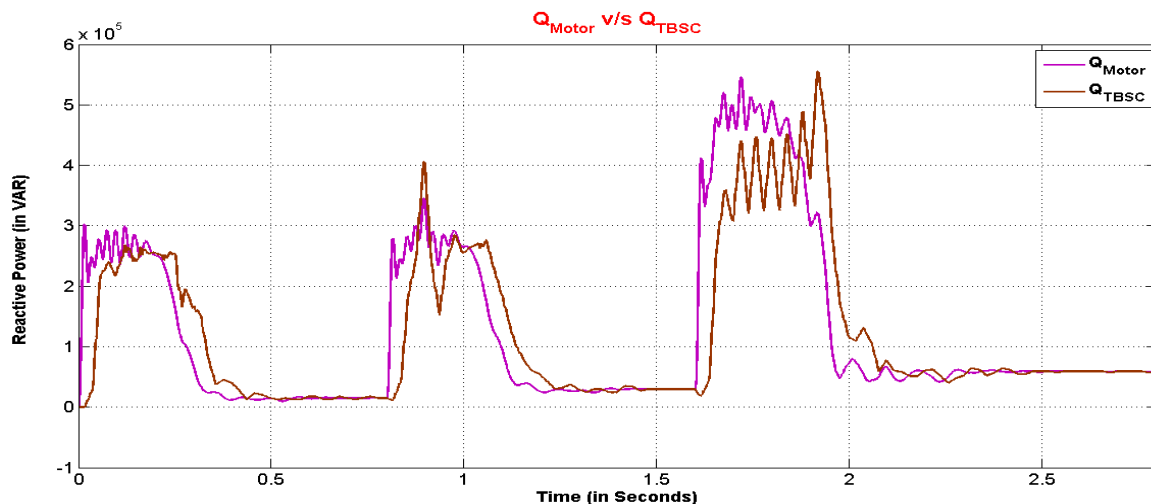


Fig. 10 shows the motor line voltage with TBSC compensator. When I.M.1 is switched on at  $t = 0$ sec, motor line voltage drops to 389V i.e. small voltage sag of 2.01% takes place for a duration of 0.4sec. Line voltage returns to steady value of 400V in 0.4sec. When I.M.2 is switched on at  $t = 0.8$ sec, the motor line voltage drops to 377V i.e. voltage sag of 5.3% takes place for a duration of 0.4 sec. steady value of 396V in 0.4sec. When I.M.3 is switched on at  $t = 1.6$ sec, the motor line voltage drops to 360V i.e. voltage sag of 7.92% takes place for a duration of 0.65 sec. Line voltage returns to steady value of 391V in 0.7sec.

These results show that with TBSC compensator there is considerable reduction in voltage sag and there is improvement in the voltage profile. Fig.11 shows the comparison of motor line voltage with and without TBSC compensator Current waveforms through all TSC banks & which are free from harmonics and have negligibly small transients only at few switching instants.

**Fig. 10 Motor Line Voltage with TBSC compensator**

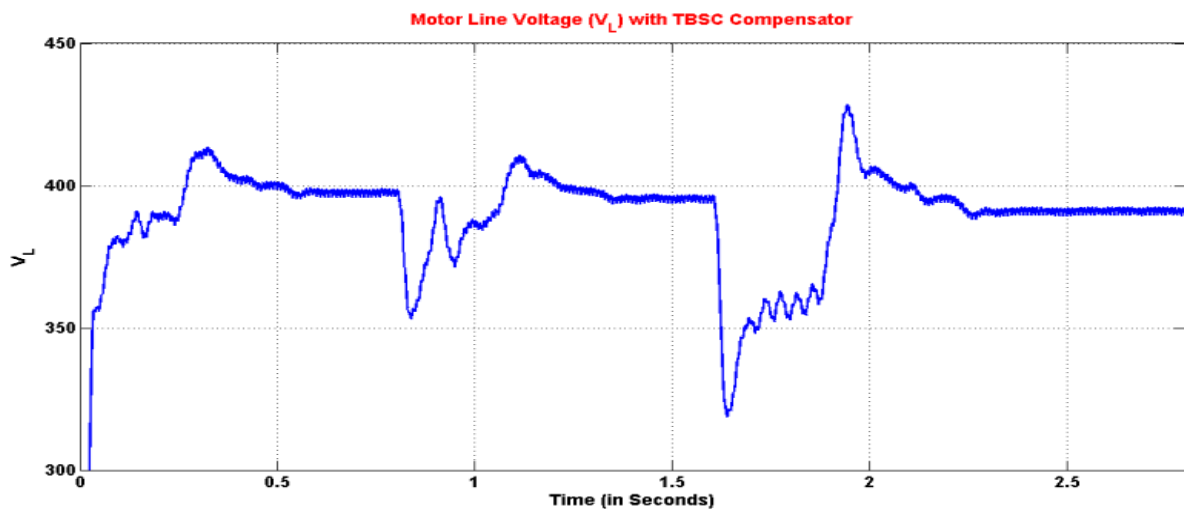
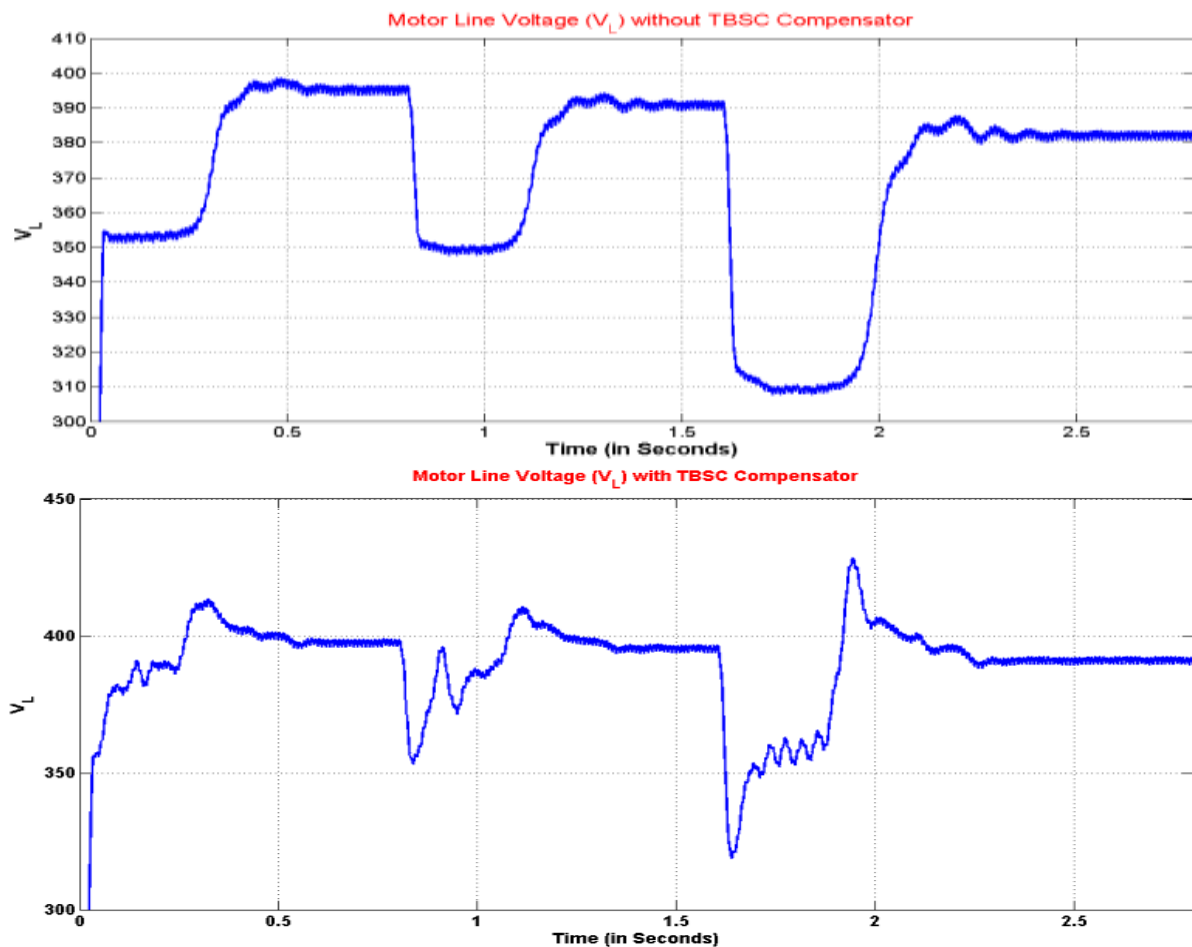


**Fig.3.12 Motor Line Voltage without TBSC compensator (Top) and with TBSC compensator (Bottom).**



#### F. Comparisons of results with & without TBSC Compensator

The simulation results are compared with and without TBSC compensator and are tabulated in the Table number IV. The comparison has been carried out based on switching instant, % Voltage sag, reactive power at starting and starting current. It shows clearly that around 12% voltage sag mitigation takes place.

**Table IV**

| Sr. No. | Parameter                           | Without TBSC Compensator |                    |                     | With TBSC Compensator                   |                    |                     |
|---------|-------------------------------------|--------------------------|--------------------|---------------------|-----------------------------------------|--------------------|---------------------|
|         |                                     | I.M.1<br>(50 h.p.)       | I.M.2<br>(50 h.p.) | I.M.3<br>(100 h.p.) | I.M.1<br>(50 h.p.)                      | I.M.2<br>(50 h.p.) | I.M.3<br>(100 h.p.) |
| 1       | Switching instant (in sec)          | 0.0                      | 0.8                | 1.6                 | 0.0                                     | 0.8                | 1.6                 |
| 2       | % Voltage sag                       | 11.14                    | 11.64              | 21.77               | 2.01                                    | 5.3                | 7.92                |
| 3       | Reactive power at starting(in KVAR) | 250                      | 250                | 380                 | Closely matches with the required value |                    |                     |
| 4       | Starting current (in A)             | 500                      | 500                | 1000                | 300                                     | 300                | 700                 |

#### IV. Conclusiona

##### A. Conclusion based on TBSC Compensator for Fast Varying Dynamic Load simulation:

A topology using a TBSC has been presented. The TSC bank step values are chosen in binary sequence weights to make the resolution small. Current flowing through TBSC as well as source is transient free. Harmonic content in source current is negligibly small. By coordinating the control of TBSC, it is possible to obtain fully stepless control of reactive power. Also one can operate the system at any desired power factor. Proposed topology can compensate for rapid variation in reactive power on cycle to cycle basis. An attempt is made through this work to develop a scheme with thyristors to reduce the cost by avoiding IGBT's and IGCT's, technically sound with reliable performance during both steady state and transient conditions, suitable for rapidly changing / fluctuating loads such as arc furnaces, tractions loads, welding equipment's etc., and self-regulating operations are practically both transient and harmonics free. The scheme developed is most suitable for highly nonlinear, fluctuating and harmonic generating loads. It gives following benefits:

- Maintaining the power factor at unity.
- Minimum feeder current and loss reduction.
- Improvement in distribution feeder efficiency.
- Improvement in the voltage at load end.
- Relief in maximum demand and effective utilization of transformer capacity.
  - Saving in monthly bill due to reduction in penalty on account of poor power factor, and reduction in maximum demand charges.
- Conservation of energy takes place..

##### B. Conclusion based on TBSC Compensator for Induction Motor Load simulation:

A topology for direct online starting of induction motors using TBSC compensator is presented. TSC bank step values are chosen in binary sequence weights to make the resolution small in order to achieve almost stepless reactive power compensation. Harmonic contents in source current are negligibly small. With the use of TBSC compensator; voltage sag magnitude gets reduced as well as voltage profile is improved. Controller operates in a closed loop to determine the number of capacitor units to be switched in the system. At the time of starting of I.M.s higher capacitor banks are switched in the system while once the motor reaches the rated speed only few lower capacitor banks will remain connected at the PCC. Thus at all times power factor is maintained near unity. The proposed scheme is effective during both steady state and transient conditions. Separate starting method for individual induction motors can be avoided and many motors can be started direct online using the proposed scheme as long as TBSC banks are capable of supplying the required reactive power demand.

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