



Modelling and Simulation of Low Power SRAM Cell with Improved Read Speed at 45nm Technology

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Abstract: Read stability and read speed in SRAM cell are most likely problems in SRAM. Access transistors used to access the basic latch consumes unwanted time to read the cell during read operation, moreover external noise may corrupt the cell data. To overcome this problem the 10T SRAM cell design has been introduced in this research work. The paper here focuses on the analysis of read behaviour of the cell structure using cadence tool at 45nm technology, and compared with the reported basic 6T structure. While the conventional 6T SRAM cell is equipped with word line for both read and write access, the 10T SRAM cell here uses a different read enable line to read the stored bit. This allows the memory element to remain isolated from the external disturbance, in addition to this, the additional time required to activate the access transistors is not required as the read operation in this cell does not require it.

Keywords: SRAM Cell, High Speed, Read Stability, Low Power.

I. Introduction

The SRAM topology proposed in this paper uses 10T structure to produce a faster read operation without disturbing the cell [1]. The conventional 6T SRAM as shown in figure 1 uses word line to access the latch for reading as well as writing operation, where read operation requires additional time to activate the access transistors which decreases the speed of the cell. Slow read operation in SRAM means time required to respond to read operation would be large. As a result, the leakage power over this long period of time in the circuit would increase. Also, access transistors may introduce external noise which may corrupt the data of the cell. These problems make the SRAM structure unsuitable for practical applications.

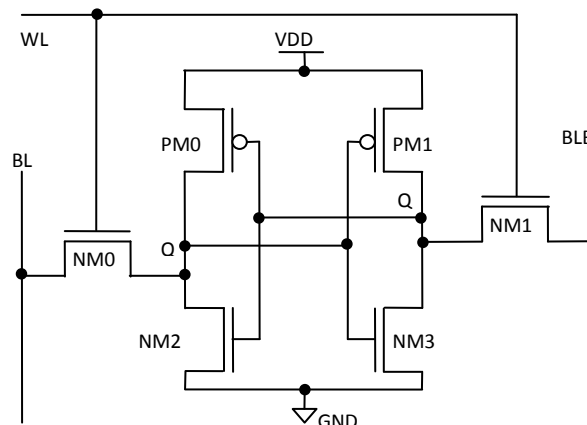


Figure 1. Conventional 6T SRAM Cell.

To address these issues, the research work here introduces a 10T structure cell as shown in figure 2 which limits the use of access transistors during read operation. This result in skipping the time required to activate the access transistors thus increasing the speed of response of the read operation.

II. The 10T SRAM Cell

In addition to the conventional 6T structure, the new 10T cell consists of 4 more MOSFETs which solely participate during read operation. The use of access transistors is thus not required while reading the cell. The SRAM cell structure is required to have high speed performance and high noise immunity. The design thus fulfils the two objectives of improving the speed as well as increasing the static noise margin [2] [4]. The buffer-inverter structure as shown in figure 2 helps in fast read operation as no activation of access transistors is

required. This structure isolates the basic latch from external noise as access transistors are off, hence the noise immunity of the cell would also be improved. Improved speed performance would reduce the power consumption which was due to long read operation. Thus power consumption of the cell is also reduced to a significant level.

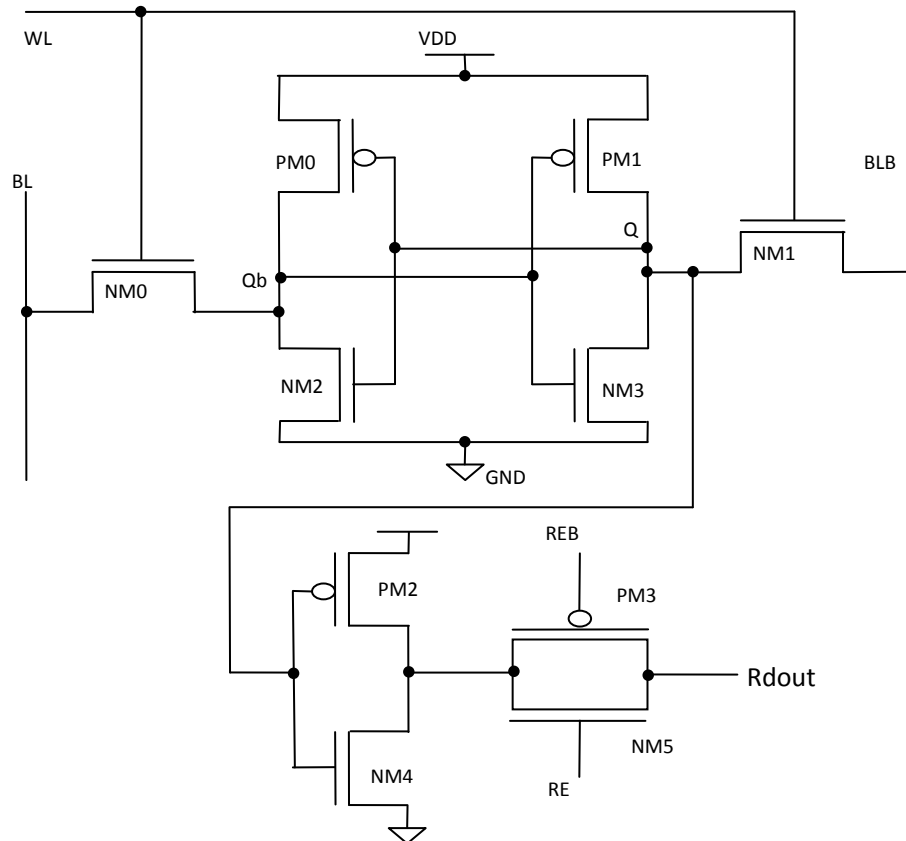


Figure 2. The 10T SRAM Cell.

When the cell is operated under write mode it works similar to that of the conventional 6T structure. The word line is asserted high so that the access transistors become active and the data to be written is given on the bit lines. After the latch stores the required data, the word line is pulled low and the access transistors go off. This isolates the latch from external circuit. The read operation, unlike the conventional 6T cell structure, is different for the 10T SRAM cell. The 10T cell employs an inverter as read buffer [3]. For read operation no word line assertion is required which reduces the excess time to activate the access transistors. To read the data from the 10T structure, simply the read lines are asserted high the data appears out on the Rdout line, thus making the read operation faster. The read waveform for the 10T SRAM cell is shown in figure 4.

The layout of the new 10T SRAM structure has been designed using Cadence Virtuoso tool with the aim of minimum area requirement. This makes the cell more efficient in terms of area as well as power. Figure 3 shows the layout of 10T SRAM cell.

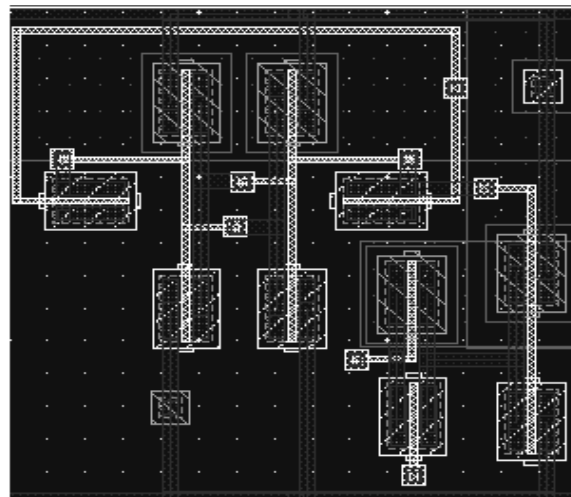


Figure 3. Layout of 10T SRAM Cell.

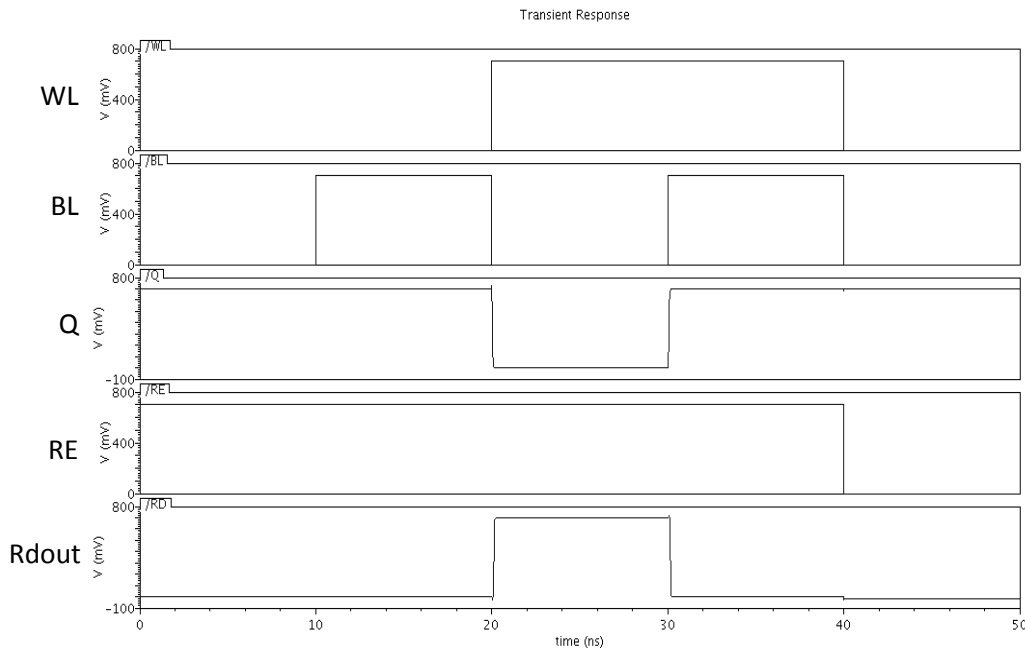


Figure 4. Read Waveform of 10T SRAM Cell.

Since the inverter is connected with memory element prior to access transistor, it provides the read operation independent of access transistors as shown in waveform. Read enable (RE) and read enable bar (REB) have been used which are kept at opposite voltages and read operation takes place when RE becomes high therefore read cycle depends on read enable and read enable bar. This makes the operation of circuit independent of bit lines whereas it depends on read lines and gives disturb free read operation. The read delay in the circuit is calculated as 50 ps.

III. Power Consumption

Some parameters such as sub-threshold leakage, temperature and larger supply voltage [7] [9] [12] (V_{dd}) impose a greater impact on power consumption in any circuit. 10T SRAM cell has reduced sub-threshold leakage as compared to the 6T SRAM cell due to the read-disturb free circuit. In the read cycle, delay and leakage reduces as the disturb free circuit is connected to output node Q before the access transistor hence making the read operation independent of access transistors and bit lines. This reduces a significant amount of leakage current which could have been due to access transistors. The drain current equation for MOSFET can be given as:

$$I_D \approx I_{D0} e^{\frac{V_{GS} - V_{TH}}{nV_T}} \quad (1)$$

Where V_{GS} = Gate to Source Voltage

V_{TH} = Thermal Voltage or Volt equivalent of temperature

I_{D0} = Dark Current or Leakage Current

$$n = 1 + C_D / C_{OX}$$

C_D = Capacitance of depletion layer

C_{OX} = Capacitance of oxide layer

Thus at $V_{GS} \leq V_{TH}$ The drain current will be nearly equal to leakage current flowing through the MOSFET. This current increases the power consumption of the transistor even when it is in cut-off state.

Figure 5 shows the currents of all the four transistors of latch in 6T the SRAM cell where as figure 6 illustrate these currents for 10T SRAM cell. From figure values it is clear that the leakage has been reduced in 10T structure as compared to 6T structure. From 1 it is also clear that if temperature is increased thermal voltage will also increase which increases the power consumption. Moreover increasing the supply voltage may also increase the power consumption of the cell. The 10T SRAM cell structure has therefore been tested for variation of power consumption against temperature and supply voltage respectively to verify that the structure consumes power still in nano-Watt range. The overall circuit leakage power is reduced to 19.09 nW. Figure 7 shows power versus temperature curve for 10T structure whereas the variation of power against supply voltage V_{dd} has been illustrated in figure 8. These figures confirm the power stability of the cell even at raised temperature and supply voltage. Fig. 7 shows the leakage power waveform of 10T SRAM cell.

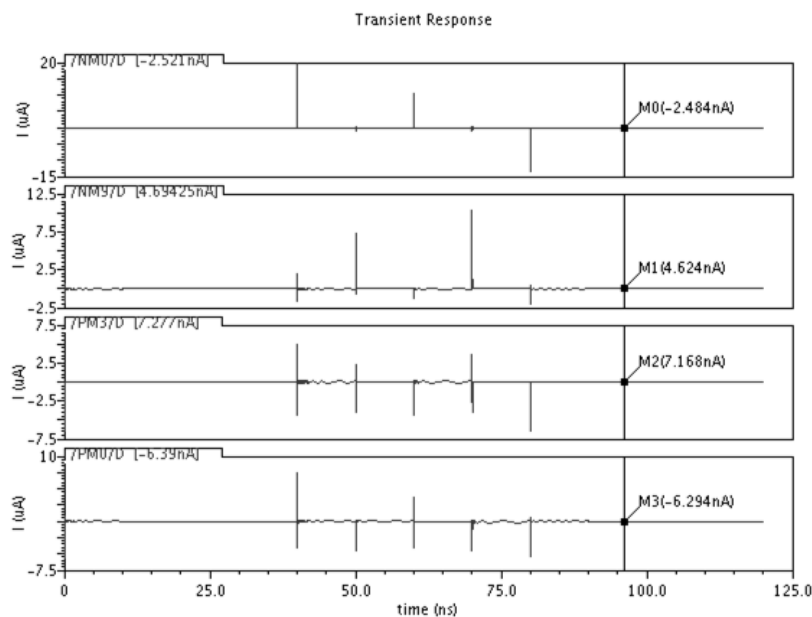


Figure 5. Leakage current waveform of 6T SRAM Cell.

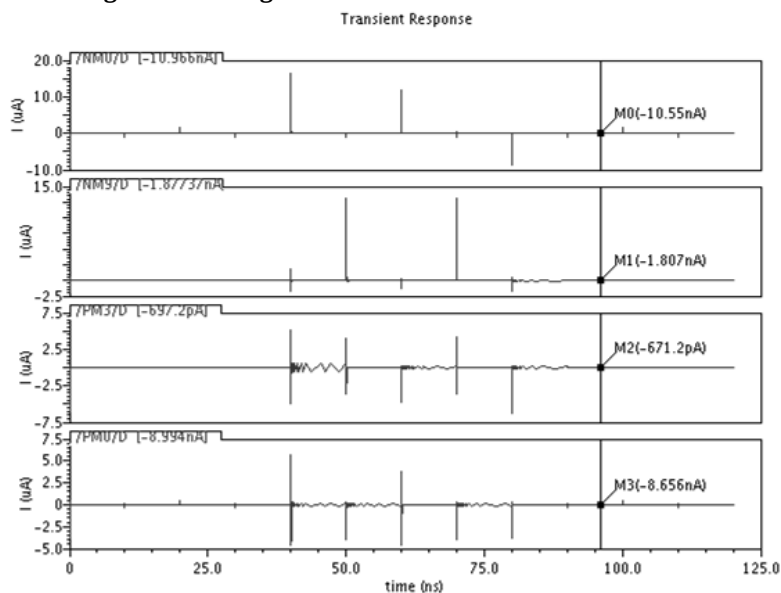


Figure 6. Leakage current waveform of 10T SRAM Cell.

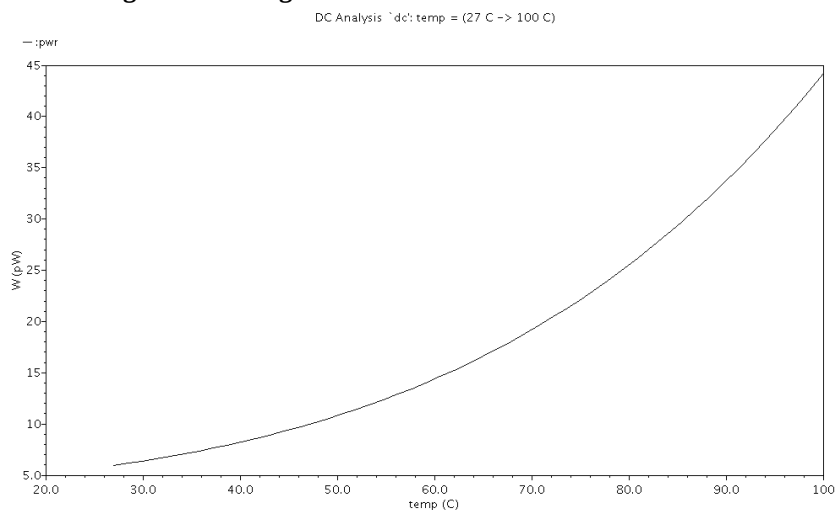


Figure 7. Power versus Temperature Curve of 10T SRAM Cell.

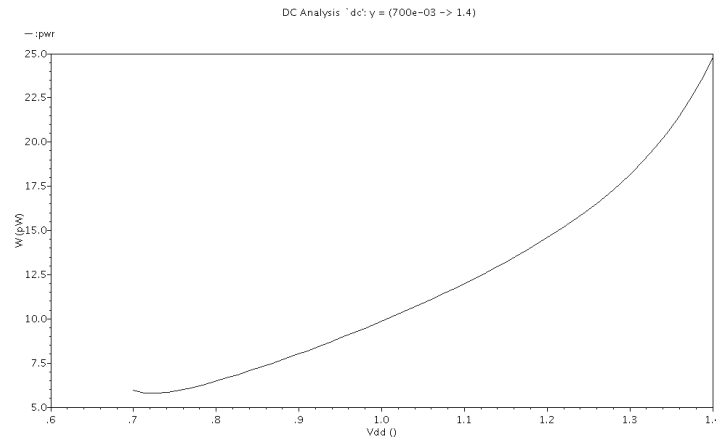


Figure 8. Power versus V_{dd} Curve of 10T SRAM Cell.

IV. Simulation Results

Table 1. Results for 6T and 10T SRAM Cell

Parameter	6T SRAM	10T SRAM cell
Technology	45nm	45nm
Voltage supply	700 mV	700 mV
Read delay	110 ps	50 ps
Power	19.09 nW	12.09 nW

V. Conclusion

The SRAM cell here has been simulated using Cadence Virtuoso tool at 45nm technology. These results are compared with the performance results of the conventional 6T SRAM cell. With the accomplishment of the objectives of the research work, the results reveal that 10T SRAM cell consisting a read disturb free circuit improves the read delay and increases the SNM of the cell hence provides better performance and high speed. The power consumption of 10T structure has also been analyzed by varying the temperature and supply voltage of the cell which shows stable and desired level of power consumption. Results discussed here confirm that 10T SRAM cell would be a better choice as compared to 6T SRAM cell for disturb free operation in future practices.

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