



Design and Analysis of Hybrid Current/Voltage CMOS SRAM Sense Amplifier with Offset Cancellation

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Abstract: In a hybrid current/Voltage Sense amplifier both current and Voltage sensing techniques are used which makes it a better choice than a conventional current or voltage sense amplifiers. The hybrid current/Voltage Sense amplifier works in three phases (1) Offset cancellation (2) Access phase (3) Evaluation phase. The offset cancellation is done simultaneously with word line decoding, so as to speed up the process. The hybrid sense amplifier works in three phases-Offset cancellation (200ps), Access phase (300ps) and Evaluation phase. The sense amplifier is analyzed with a column of 512 SRAM cells at 180nm technology node and compared to CMOS conventional Voltage sense amplifier. The sensing range of the hybrid sense amplifier is improved from 1.18mV to 92mV, with a very less consumption of energy, about 6.84fJ. This sense amplifier is analyzed with a column of 512 SRAM cells at 180nm technology node and compared to CMOS conventional voltage sense amplifier. Further this architecture is implemented and compared to CMOS conventional Voltage Sense Amplifier at 130nm and 90nm technology nodes.

Index Terms: Static random access memories (SRAM), Pre sense amplifier (PSA), Voltage Sense Amplifier (VSA), Current Sense Amplifier (CSA), Precharge, Offset cancellation.

I. INTRODUCTION

Sense amplifiers are the memory peripherals, their use in Static Random Access Memory improves the speed and area consideration. In an integrated circuit a memory is attached to number of peripherals which wants to use the content of the memory, but the potential developed at the output terminals of the memory (SRAM) is too low to drive the peripheral circuitry, hence the need of a sense amplifier comes into picture. It senses such a low signal and drives the peripheral. There are number of architectures for a Sense amplifier that are being used, voltage sense amplifiers or current sense amplifiers but this paper highlights a hybrid current/voltage sense amplifier which uses both current as well as voltage sensing technique.

VSA (voltage sense amplifier) is a latch, made with two cross coupled CMOS inverters, providing full voltage swing (0 to V_{dd}) at the output terminals with very less voltage at the input nodes. Keeping in mind that the voltage at the input of VSA should be greater than the offset for correct results and proper detection. If this is not the case then the bit line voltage swing becomes larger and directly affects the speed, power as well as the word line activation time. This architecture is a popular choice due to its simple design. Moreover it is differential type circuit same as that of a 6T SRAM cell, so it can be directly and easily used with the SRAM cell. CSA (current sense amplifier) are generally used for high speed applications. The voltage swing required for CSA's for correct detection is not large. In this case the current creates a variation in the charge resulting in a large voltage at the output. Having both the advantages of VSA and CSA, this paper showcases a Hybrid Current/Voltage sensing scheme with offset cancellation and a reduction in word line activation time [1-6].

II. WORKING OF SENSE AMPLIFIER

Hybrid current/ voltage sense amplifier operates in three following phases 1) Pre amplifier Offset cancellation phase (POC) 2) Access phase (ACC) 3) Evaluation phase. The offset is already canceled in the POC phase, during the ACC phase the CSA plays its part and its output is amplified by the VSA in the Evaluation phase. There is a PSA (pre sense amplifier) in the circuit which acts as the CSA. Transistors M1 and M2 acts as PSA, the bit lines, BIT and BITB are the inputs of the PSA.

A And A BAR is the outputs of the PSA. There is a mismatch in the threshold voltage of M1 and M2, which creates a difference in the effective voltage (v_{eff}), given by $v_{gs} - v_t$, which in turn creates a difference in the transconductance (g_m) because g_m is a function of v_{eff} . this results in the PSA differential offset [7]. To overcome this problem the transconductance of the transistors should made equal. In the offset cancellation

phase (POC) the offset is cancelled by making the bit lines charge to an equal potential. The precharge voltage is about 900mv. During this phase the word line is inactive where as the sense and senseb signals are active, the output terminals of M3 and M4 are tied to v_{dd} . The transistor having less v_t creates a larger voltage on the respective word line because it sources more current. At the end of POC phase a potential gets developed between the BL and BL bar lines and the effective voltages of M1 and M2 are equalized. The circuit enters into next phase, the ACC phase, where the word line gets activated and the senseb signal is deactivated. A differential voltage is created at the input of VSA (SA and SA Bar), which is larger than bit lines because the capacitance of A and A Bar is far less than the capacitance of Bit lines. The third phase is the evaluation phase, it starts when the amplifier signal goes high (amplifier = 1). The correct results will only be obtained if the voltage at the input of VSA is greater than its offset, hence $\Delta v_{out} > v_{off} - v_{SA}$.

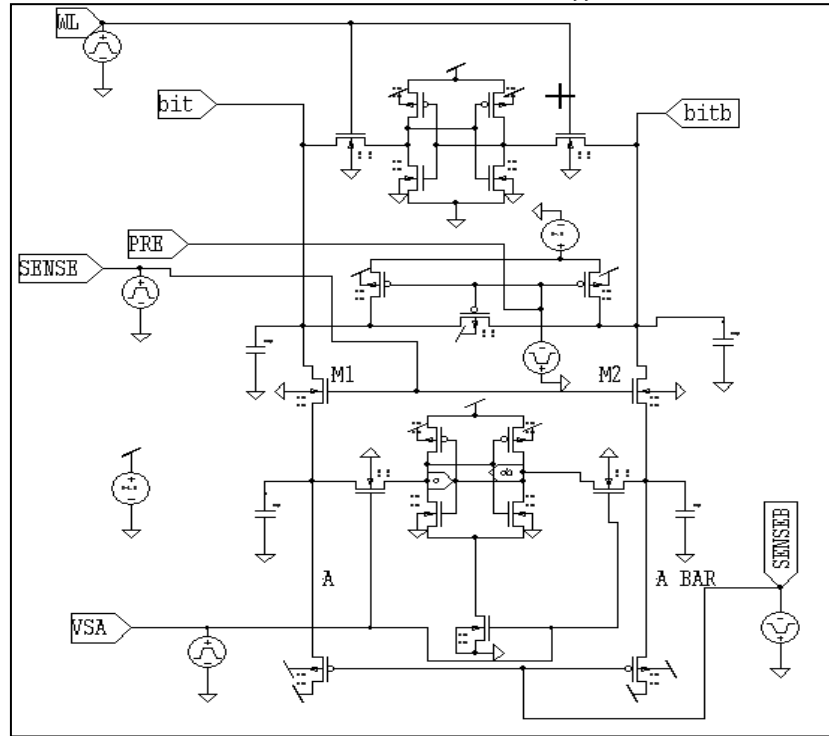


Fig. 1: Hybrid Sense amplifier with 6T SRAM Cell and Precharge circuit.

In totality if a better by making POC phase longer, better offset cancellation can be obtained. In this architecture the word line activation time is also reduced. The offset cancellation phase lasts only for 200ps i.e. ($T_{POC} = 200ps$) and the Access phase is for 300ps i.e. ($T_{ACC} = 300ps$). The precharge voltage (V_{pre}) is .9v and the bitlines are allowed to precharge only a few millivolts more than .9v through the source of transistors M1 and M2 only during the offset cancellation phase. During this POC phase both the voltages at bit lines try to become equal and no differential voltage termed as offset is created at the end of POC phase. At the end of Access phase i.e. after 500ps, a differential voltage of about 1mv is developed at the bit lines and a differential voltage of about 92mv is also created at the input nodes of Voltage Sense Amplifier. In the Access phase the charging of bit lines is still there but the bit line differential voltage drops during this phase because the CSA is made from only nmos and the input impedance of these transistors is not zero (idle case). In this scheme the Access time is shorter which leads to high stability of the cell and the precharging is done at more than half of the biasing voltage hence the data is not lost [2].

III. ANALYTICAL EXPRESSIONS / CALCULATIONS

Following is the flow chart showing all the three phases of the Hybrid Current Voltage Sense amplifier:

The analysis of the circuit is done on the basis of certain mathematical expressions described as follows: [2]

The transconductance of PSA is given by

$$g_m = \mu_n C_{ox} \frac{W}{L} \times \frac{V_{dd} - V_{pre} - V_t}{(V_{dd} - V_{pre} - V_t)AT_{POC} + 1} \quad (1)$$

Where A is given by

$$A = \mu_n C_{ox} \frac{W}{2LC_{BL}} \quad (C_{BL} \text{ is the bit line capacitance}) \quad (2)$$

Transconductance depends on the gate and source voltages of the Pre sense amplifier transistors.

A residual offset voltage at the end of access phase carried from the POC phase can be calculated as follows

$$V_{OS-PSA} = g_m \times \frac{T_{ACC}}{C_p} \times V_{OS-RES}(T_{POC}) \quad (3)$$

Where C_p stands for parasitic capacitance

Differential voltage at the output of PSA created due to the cell current (I_{cell}) over the Access phase is given by

$$\Delta V_{cell} = \int_0^{T_{ACC}} \frac{g_{m1_{cell}}}{C_p C_{BL}} t dt = \frac{g_{m1_{cell}} T_{ACC}^2}{2 C_p C_{BL}} \quad (4)$$

Now the differential voltage at the input nodes of VSA is given by

$$\Delta V_{VSA} = \Delta V_{cell} - V_{OS-PSA} \quad (5)$$

For correct detection

$$\Delta V_{cell} > V_{OS-PSA} \quad (6)$$

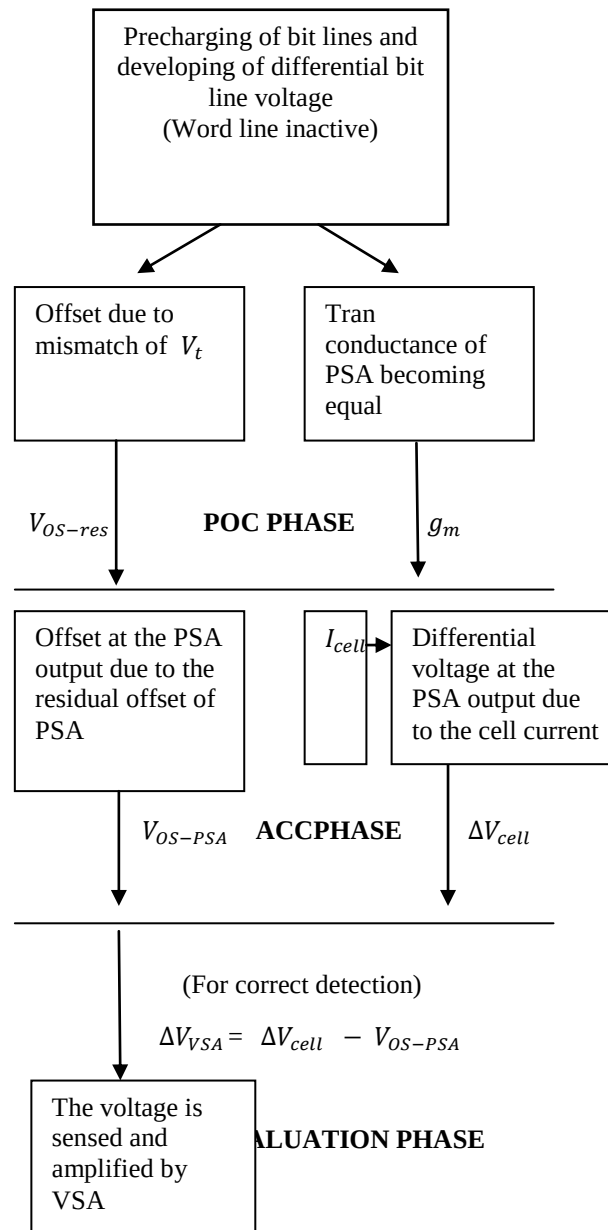


Fig. 2 Flow chart showing different phases of Hybrid Sense Amplifier

In this scheme the bit line capacitance, $C_{BL} = 1\text{pf}$ and cell current, $I_{cell} = 42.76\mu\text{A}$ for a configuration of 512 cells/column for .18 technology with $V_{dd} = 1.8\text{V}$.

Minimum offset cancellation time required for a given Access time is given by

$$T_{POC-min} = \frac{\sqrt{2C_{BL}\Delta V_T}}{\sqrt{I_{cell}T_{ACC}}} - 1 \times \frac{1}{(V_{dd} - V_{pre} - V_T)A} \quad (7)$$

IV. RESULTS AND COMPARISON

In this section CMOS conventional Voltage Sense Amplifier is compared with the hybrid current/Voltage Sense Amplifier. Both the architectures are analyzed at 180nm technology and are also implemented on technologies like 130nm and 90nm.

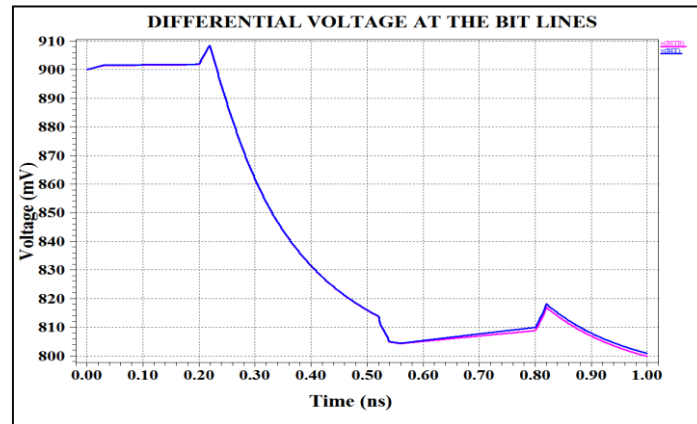


Fig. 3: Differential voltages at the bit lines

Hybrid current/Voltage Sense Amplifier is implemented at 180nm and the bit lines are precharged at 900mV. M1 has more threshold voltage than M2, hence bitb line charges slowly than bit line. At the end of POC phase(200ps) both the bit lines gets precharged to an equal voltage with a negligible offset of $149.31 \mu V$. The bit lines are precharged by the Pre sense Amplifier in the ACC phase as well but as seen from the following figure there is a drop in potential due to the input impedance of the CSA. After the ACC phase (500ps) a differential voltage of about 1.18mV is developed on the bit lines and a differential voltage of about 92mV is developed at the input of VSA.

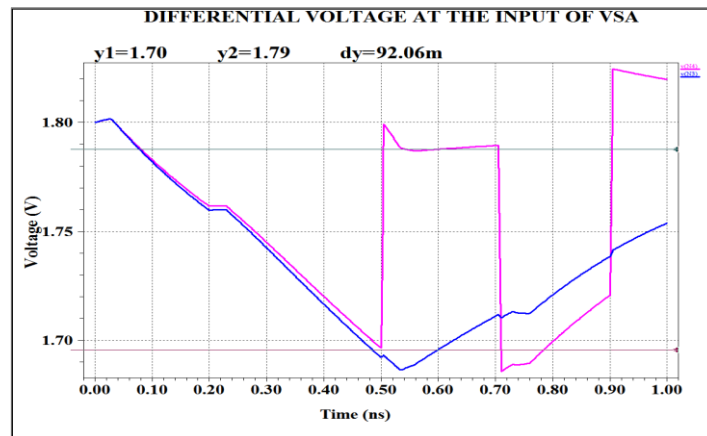


Fig. 4: Differential voltages at the Input of VSA

Corresponding to this potential of about 92mV at the input of VSA, the voltage swing measured at node “o” of the VSA is (1.74 to 1.86) v as shown in figure 4. The final voltage at one output node of the VSA reaches V_{dd} and at the other node reaches zero.

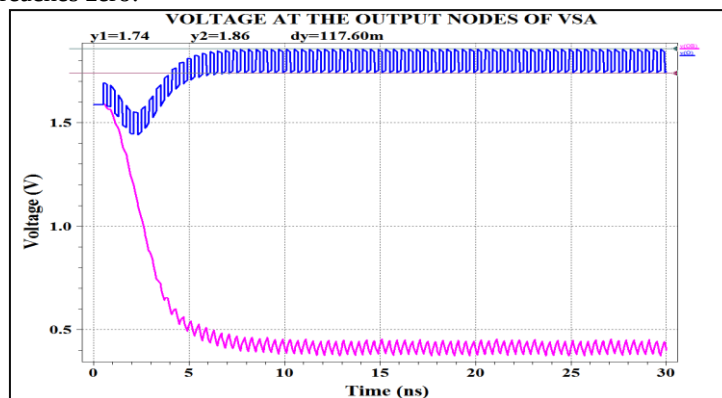


Fig. 5: Voltages at the output of VSA.

The minimum and maximum power of the circuit is shown in the following waveform:

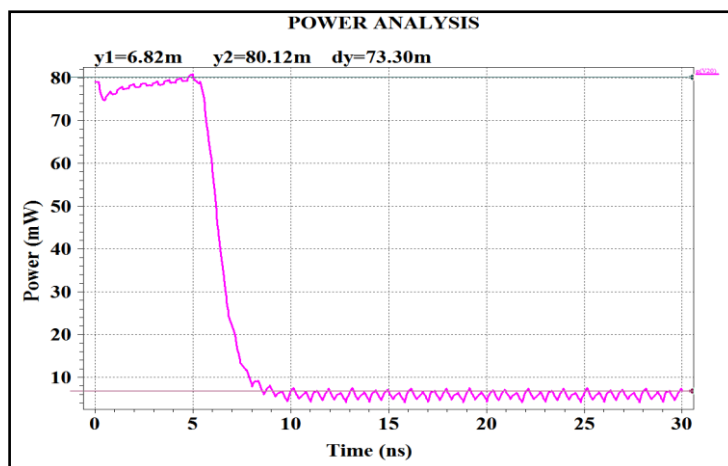


Fig. 6: Power analysis of the circuit.

Max power= 80mw and Min power= 6.28mw

CMOS Conventional Voltage Sense Amplifier is analyzed at 180nm and compared with the hybrid current/Voltage Sense Amplifier.

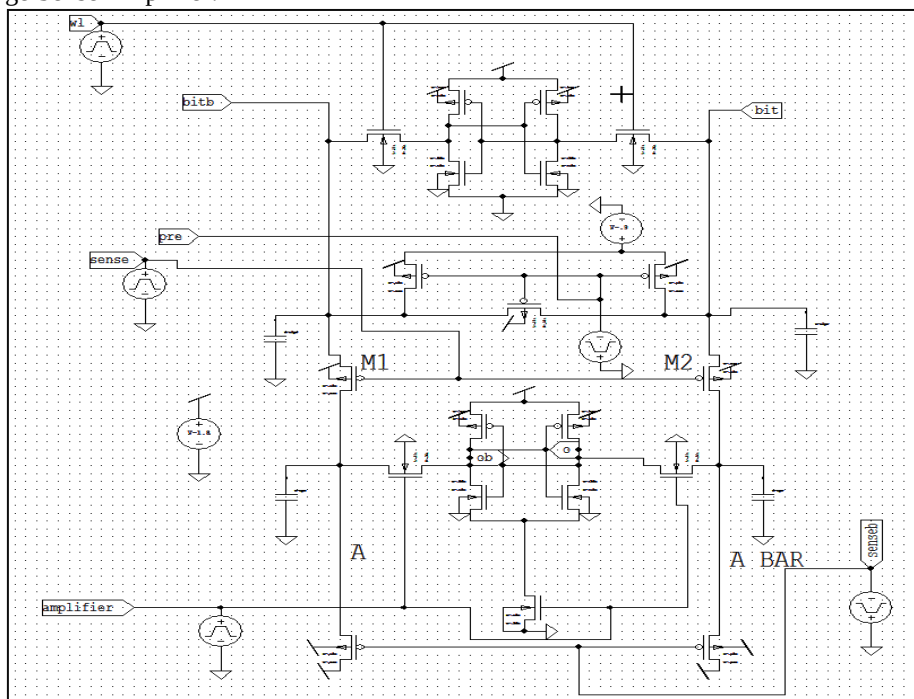


Fig. 7: CMOS Conventional Voltage Sense Amplifier with 6T SRAM Cell and Precharge circuit.

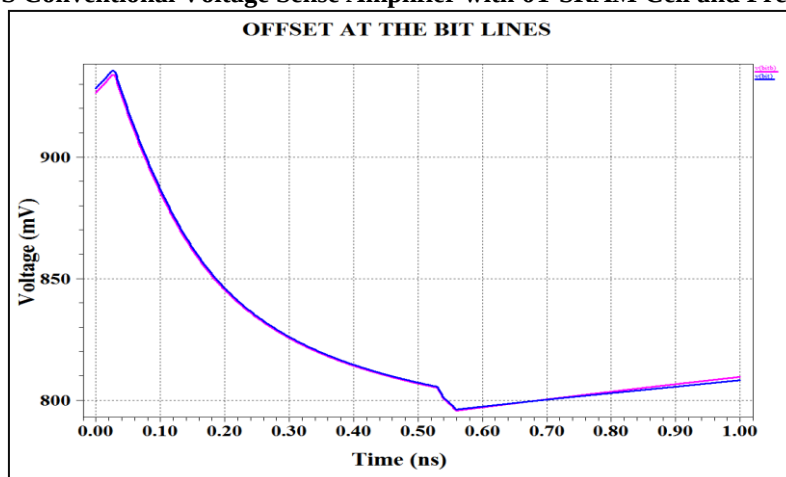


Fig. 8: Offset voltages at the Bit Lines of CMOS Conventional VSA.

Both the bit lines are precharged at 900mv and they keeps on precharging up to about 935mv,a differential voltage is developed on the bit lines which is termed as offset because there is no provision of offset cancellation, hence the offset in this case is about 1.68mv.

Differential Voltage developed at the bit lines of the CMOS conventional VSA is as shown in figure 8, the difference in potential raises after 2ns.

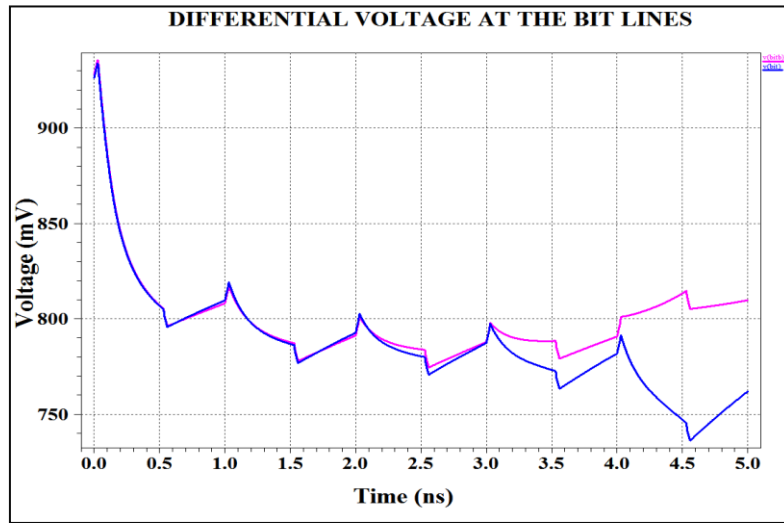


Fig. 9: Differential Voltages at the bit lines.

After the ACC phase (500ps) a differential voltage of about 65.87 is developed at the input of VSA as shown in figure 9.

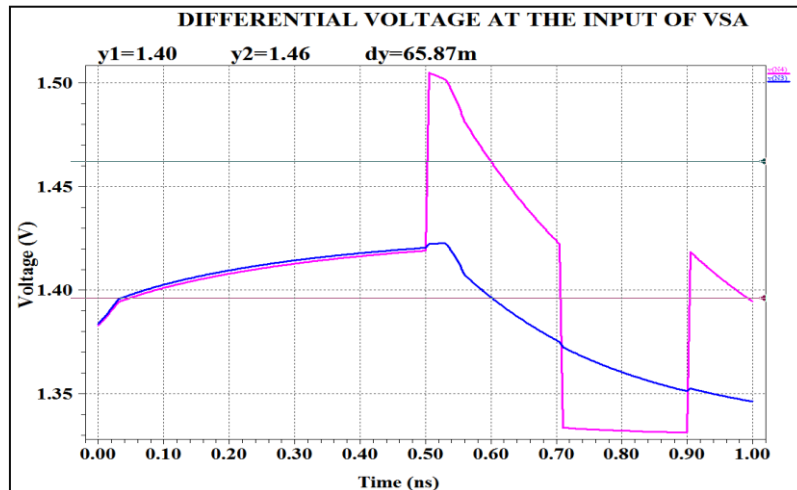


Fig. 10 Differential Voltages at the input of VSA after the ACC phase.

Final output at "o" and "ob" nodes of CMOS conventional VSA is shown in figure 10. The voltage swing measured at node "o" of the VSA is (1.60 to 1.75) v and the voltage at other node voltages goes to zero.

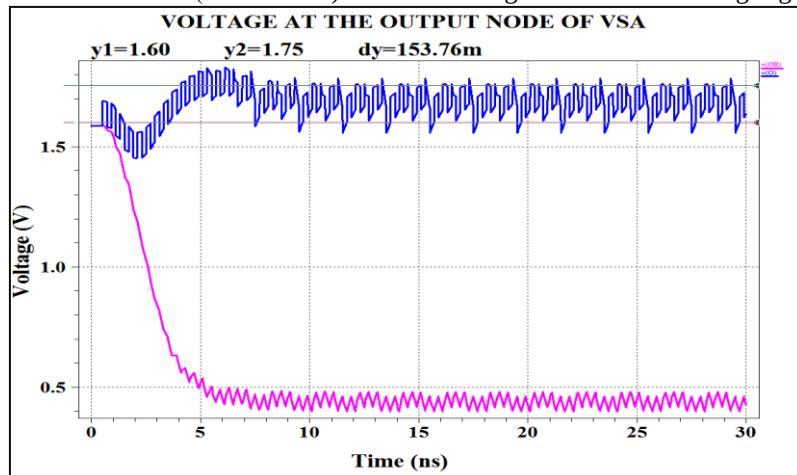


Fig. 11: Voltages at the Output Nodes of VSA.

The minimum and maximum power of the CMOS Conventional VSA is shown in the following waveform:

Max power= 81.43mw

Min power= 6.86mw

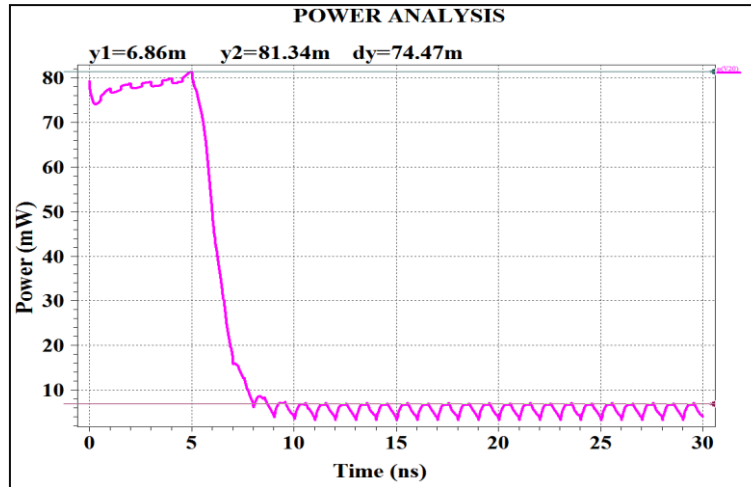


Fig. 12: Power analysis of the circuit.

All the results discussed above are tabulated as follow

Table: 1 Comparison at 180nm

Specifications	CMOS Conventional VSA	Hybrid Current/Voltage Sense Amplifier
Precharge Voltage	900mV	900mV
Sensing Range (Upper - lower)	65.87mV(upper sensing range)	1.18mv-92mV
Offset	1.68mV	149.31 μ V
Energy consumption	3.06fj	6.84fj
Output Voltage Swing	1.75v to1.60v	1.86v to 1.74v
Access Time	500ps	300ps
Power	Maxpower= 81.43mw Minpower= 6.86mw	Maxpower= 80mw Minpower= 6.28mw

The energy consumption of the Hybrid current /Voltage sense amplifier is given by:

$$E_{bl} = 2 \times C_{BL} \times V_{DD} \times (V_{BL}(T_{POC}) - V_{PRE})$$

The precharge voltage should be chosen such a way that it has to be equal or more than half of the bias voltage. Increasing the precharge voltage can lead to decrease in the energy consumption but if we want to have the overall timing head to be less than the T_{ACC} of CMOS conventional method, then we need a very less precharge voltage but lowering the precharge would lead to more power consumption and affects stability on the other hand a largest precharge voltage would lead to minimum power consumption.

$$T_{Total} = T_{POC} + T_{ACC} + T_{EV} + T_{Row Decoder}$$

For a precharge of about 1.1v the offset reduces to 104 μ V and the sensing range becomes 3.25mv -89.21mv.

The energy consumption of a CMOS Conventional Voltage Sense Amplifier is given by:

$$E_{bl} = C_{BL} \times V_{DD} \times \Delta V_{BL}$$

The hybrid current/voltage Sense Amplifier and CMOS Conventional Sense Amplifier is implemented at 130nm and the results are tabulated as follow:

Table: 2 Comparisons at 130nm

Specifications	CMOS Conventional VSA	Hybrid Current/Voltage Sense Amplifier
Precharge Voltage	650mV	650mV
Sensing Range (Upper - lower)	28.8mv(upper sensing range)	405.05 μ V –37mV
Offset	1.28mV	60.27 μ V
Energy consumption	1.66fj	2.2fj
Output Voltage Swing	1.28V to 1.23V	1.32V to1.28V
Power	Maxpower= 27.66mw Minpower= 2.35mw	Maxpower= 26.63mw Minpower= 2.35mw

Further the hybrid current/voltage Sense Amplifier and CMOS Conventional Sense Amplifier is implemented at 90nm and the results are tabulated as follow:

Table: 3 Comparisons at 90nm

Specifications	CMOS Conventional VSA	Hybrid Current/Voltage Sense Amplifier
Precharge Voltage	500mV	500mV
Sensing Range (Upper - lower)	16.17mV(upper sensing range)	38.87 μ V-18.2mV
Offset	1mV	19.65 μ V
Energy consumption	1fj	.54fj
Output Voltage Swing	966mv to 941mV	1.01v to 985 mV
Power	Maxpower= 13 mw Minpower= 1.24mw	Maxpower= 12.94mw Minpower= 1.15mw

V. CONCLUSION

The hybrid voltage/current sense amplifier with 512 cells per coloumn is implemented at different technology node. The sensing range of the Hybrid Current/ Voltage Sense Amplifier has been improved to 1.18mv-92mv by precharging to a lowered potential of 900mv. Due to a less precharge voltage the energy consumption of Hybrid Current/ Voltage Sense Amplifier is lowered to few fempto joules. The Offset is almost neglgible about 141.31 μ V. The hybrid current/Voltage sense Amplifier can be implemented at 130nm and 90nm with a output potential raised to the biasing voltage.

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