



Equal Area Criterion Scheme to Reduce DC Bus Voltage Stress of Single Stage Single Switch Power Factor Corrected Converter

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Abstract: Single Stage Single Switch Power Factor converter topology is selected in such a way that input PFC stage is Discontinuous Current Mode (DCM) boost converter and output stage is Continuous Current Mode (CCM) fly back converter providing wide bandwidth response. Major problem associated with the converter is strong dependency of dc bus voltage stress with the output load. A design solution to avoid this problem is presented by suitable selection of boost inductor using Equal Area Criterion (EAC) and by implementing simple closed loop control. Design, simulated studies using Orcad and experimental verifications have been performed. Problem of voltage stress was found almost eliminated.

Keywords: EAC, S4SMR, Switch mode rectifier, power factor converter, PFC

I. Introduction

Line current harmonics are injected to the electrical network by non-linear loads connected to the network, and are multiples of 50Hz. Common examples of such devices found in industrial environments include variable frequency drives, welders, switched mode power supplies, battery chargers, UPS systems, computers, electronic lighting etc. Usually power converters use a diode rectifier followed by a bulk capacitor to convert AC voltage to DC voltage. Conventional diode rectifiers used in electronic equipment draw pulsed current from the utility line. Consequently the power factor becomes poor (0.5- 0.6) due to high harmonic distortion of the current waveform. The simple solution to improve the power factor is to add a passive filter which is usually composed of a capacitor and an inductor. However, this passive filter is bulky and inefficient since it operates at line frequency. Therefore, a power factor correction stage has to be inserted to the existing equipment to achieve a good power factor. A typical switching power supply presents a nonlinear load to the power source. The high peak current drawn from the line is due to the small conduction angle.

Since these power converters draw pulsed current from the utility line the power factor becomes poor due to high harmonic distortion of the current waveform. Therefore, a power factor correction stage has to be inserted to the existing equipment to achieve a good power factor. Several standard and review articles in the literature have addressed power quality related issues in AC to DC converters. New configurations of power factor corrections are being developed to mitigate the harmonic effects on the input line current and improve the power factor.

IEEE 519 and IEC 61000-3-2 have being developed to specify the limits of harmonic pollution levels to acceptable levels that can occur on the system. The new family of power factor corrected switching power supplies normally consists of two stages in the power circuit, viz. – The input power factor correction stage and the output DC to DC converter stage. Continuous efforts to further make these power converters compact and cost effective too lead to the development of new class of power supplies known as Single Stage Single Switch Switch Mode Rectifier, which is the integration of PFC stage and the DC to DC converter stage. It uses only one switch and controller to shape the input current and regulate the output voltage. The energy storage device in between is necessary to absorb and supply the difference between the pulsating instantaneous input power and constant output power [1].

A major problem associated with Single Stage Single Switch power factor converter is strong dependency of DC bus voltage stress across the capacitor with the output load [1], [2]. Power unbalance between PFC stage and DC-DC stage is the inherent reason for causing high DC bus voltage stress. Frequency control is other solution proposed to overcome high DC voltage stress [13]. But this call for complex control circuit. The concept of series charging,

parallel discharging capacitor scheme is another solution.[14].But this call for more component count in the power circuit

In this paper a design solution is proposed to avoid the problem of energy unbalance between energy stored during on period of switch and energy dissipated in the load by optimally sizing the boost inductor. Maximum energy stored in the inductor shall be limited to such a value that this energy matches with maximum output power required. The instant at which maximum power delivered shall be matched with the instant when the input ac voltage is at the peak. Also consider the fact that maximum power is delivered at a duty ratio which is slightly less than the limiting duty ratio (0.5) for DCM operation. Equal Area Criterion is applied between theoretically calculated fundamental component of input ac current and the peak inductor current when t_{on} is maximum. Using this approach the design was carried out, and simulated testing as well as experimental observation showed only a very small rise in DC bus voltage at light load condition, even under open loop. After introducing closed loop control with output voltage as controlled variable and duty ratio as manipulated variable the DC bus voltage stress was found almost insignificant.

II. The Bifred Converter

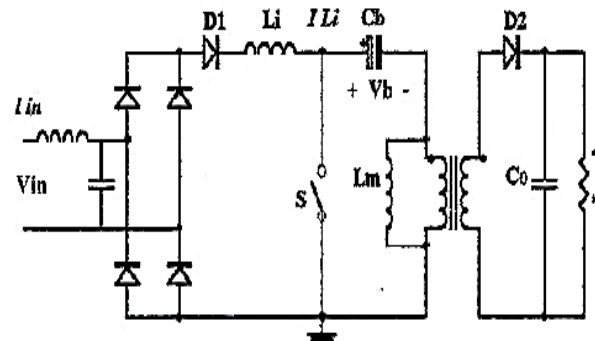


Figure 1: The BIFRED PFC ac/dc converter

One of the basic configurations of single stage single switch SMR is the BIFRED converter which is the acronym for Boost Integrated with Fly Back Rectifier / Energy storage / DC- DC converters which is shown in Fig.1.It integrates a DCM boost converter with dc-dc converter.

When S is turned on, rectified line input voltage appears across the boost inductor and the output magnetizing inductor stores their energy independently during the on interval of the switch. When the switch is turned off, the stored energies are delivered to the bulk capacitor and to the load.

Under light load condition the PFC stage without realizing this, stores the same energy as that of the heavy load leading to an unbalanced power between the input and the output [1]. This unbalanced power gets stored across the bulk capacitor causing the dc- bus voltage to increase. One way to take care of this problem is through closed loop control which will automatically reduces the on duration of the switch by sensing the output voltage thus by striking a power balance. But the dynamic response of the system being poor this method is found not so attractive [2].

III. PFC Converter With Dc Bus Voltage Feedback

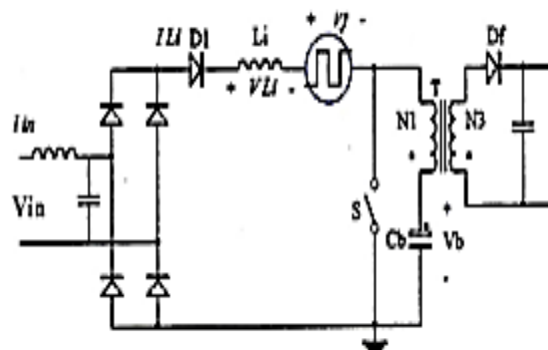


Figure 2: Converter with power stage negative feedback

An alternative method was proposed to use a negative feed back scheme in the power stage instead of in the control loop [2]. Fig 2 shows this scheme. A negative feedback voltage V_f is obtained by using a feed back winding coupled with the isolation transformer. This will make the resultant voltage available across boost inductor less when the DC-bus voltage increases, thus putting limit on to the input power drawn and by striking a power balance.

IV. The Proposed Single Stage Single Switch Pfc Converter

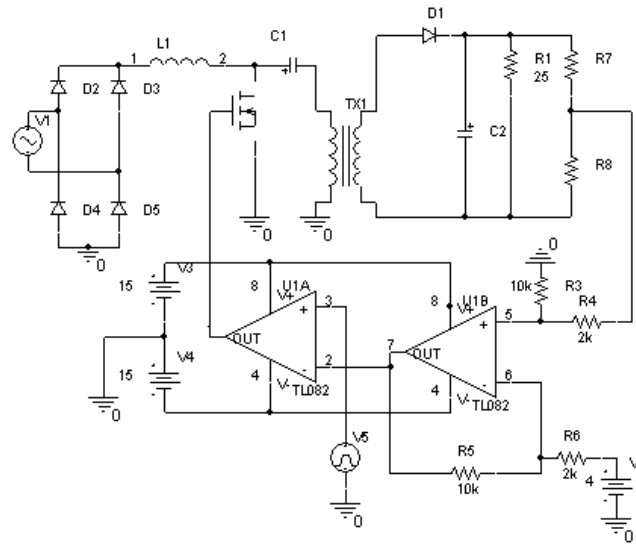


Figure 3: The Proposed Single Stage Single Switch PFC converter

Proposed converter, shown in Fig. 3, is a modified BIFRED converter, which avoids the use of $D1$ and the negative voltage feedback V_f . Equal area criterion (EAC) is applied to achieve optimum design of boost inductor, coupled with a closed loop control with output dc voltage as controlled variable and duty ratio as manipulated variable so as to eliminate the problem of dc bus voltage stress at light load.

V. Design Of PFC Stage By Equal Area Criterion.

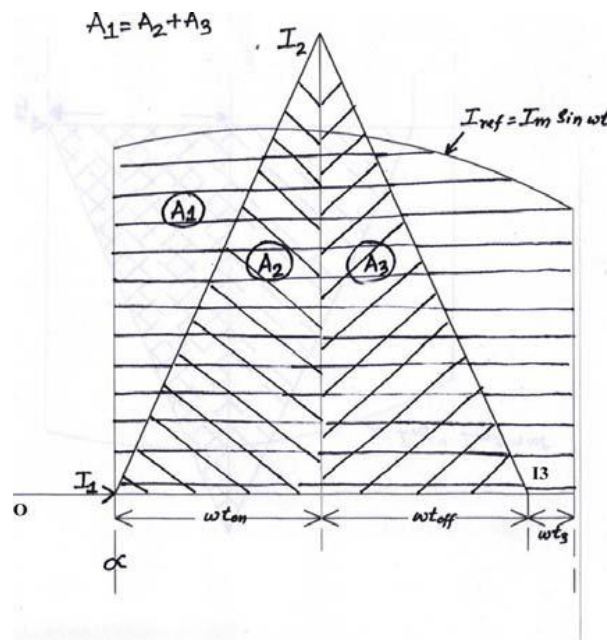


Figure 4: Input current pulse superimposed on reference current.

The rectifier input current is discontinuous in nature. A typical input current pulse superimposed on the reference current $I_m \sin \omega t$, is shown in Fig. 4.

$$T = t_{on} + t_{off} + t_3$$

ω_{ton} - On period of boost switch.

ω_{toff} - Off period of boost switch.

ω_{t3} - Non-conducting period (dead period).

α - Instantaneous switching angle

EAC applied to single stage single switch power factor converter means equalizing the area under a sinusoidal reference current and the area under the input current in the total period of one switching cycle [4].

A. EAC applied to design of boost inductor for the proposed single stage single switch power factor converter

Magnitude of the reference current is selected such a way that-

$$P_{out} = V_{rms} \times I_{rms \cdot ref}$$

Instantaneous current i_r in on mode of boost switch is,

$$i_r = I_1 + \frac{E_m}{\omega L_1} [\cos \alpha - \cos(\alpha + \omega t)] \quad (1)$$

Where $\alpha < \omega t < \omega t_{on}$

i_r in off mode,

$$i_r = I_2 + \frac{E_m}{\omega L_1} (\cos \alpha + \omega t_{on}) - \cos(\alpha + \omega t_{on} + \omega t) - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t \quad (2)$$

At the beginning $I_1 = 0$

$$\text{During on time, } i_r = \frac{E_m}{\omega L_1} [\cos \alpha - \cos(\alpha + \omega t)] \quad \text{Where } \alpha < \omega t < \omega t_{on} \quad (3)$$

Off mode current becomes zero at $\omega t = \omega t_{off}$

$$I_3 = I_2 + \frac{E_m}{\omega L_1} [\cos(\alpha + \omega t_{on}) - \cos(\alpha + \omega t_{on} + \omega t)] - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t \quad \text{Where } \alpha < \omega t < \omega t_{off} \quad (4)$$

B. Design of Boost Inductor.

At the end of on duration I_2 is maximum (I_{2peak}).

I_{2peak} occurs at $\alpha = 90^\circ$ and duty cycle is maximum. The off duration followed by this I_{2peak} will be minimum.

Value of L has to be selected in such a way that current at the end of this minimum off duration is zero.

From (3)

$$I_{2peak} = \frac{E_m}{\omega L_1} \sin \omega t_{on} \quad (5)$$

$\sin \omega t_{on} \cong \omega t_{on}$ since switching frequency is high.

$$I_{2peak} = \frac{E_m}{\omega L_1} \omega t_{on} = \frac{E_m}{L_1} t_{on} = \frac{E_m}{L_1} DT \quad (6)$$

$$L_1 = \frac{E_m}{I_{2peak}} DT \quad \text{Where } D \text{ is duty cycle} \quad (7)$$

C. DC bus voltage, output voltage and Duty ratio.

From (4), (5) with $I_3 = 0$ and assuming $\omega t_3 \cong 0$

$$0 = I_{2peak} + \frac{E_m}{\omega L_1} (-\sin \omega t_{on} + \sin \omega t_{on} + \omega t_{off}) - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t_{off} \quad (8)$$

$$0 = \frac{E_m}{\omega L_1} (\sin \omega t_{on} - \sin \omega t_{on}) + \frac{E_m}{\omega L_1} \sin(\omega t_{on} + \omega t_{off}) - \frac{(V_{dc} + nV_2)}{\omega L_1} \omega t_{off} \quad (9)$$

$$\frac{(V_{dc} + nV_2)}{L_1} t_{off} = \frac{E_m}{L_1} (t_{on} + t_{off}) \quad (10)$$

$$(V_{dc} + nV_2)(t - t_{on}) = E_m T \quad (11)$$

$$(V_{dc} + nV_2)t - (V_{dc} + nV_2)t_{on} = E_m T \quad (12)$$

$$\frac{t_{on}}{T} = \frac{(V_{dc} + nV_2 - E_m)}{(V_{dc} + nV_2)} \quad (13)$$

$$D = 1 - \frac{E_m}{(V_{dc} + nV_2)} \quad (14)$$

$$V_{dc} + nV_2 = \frac{E_m}{1-D} \quad (15)$$

VI. Design Of Output Converter Stage[8].

A. Voltage transfer function for fly back converter.

Always volt second balance should be there.

Primary Volt sec/turn= Sec volt sec/turn.

$$(V_1 - V_{swic}) \frac{DT}{N_1} = \frac{(V_2 - V_d)(1-D)T}{N_2} \quad (16)$$

$$V_2 = V_1 \frac{N_2 D}{N_1 (1-D)} \quad (17)$$

B. Voltage Transfer function of single stage single switch power factor converter

We can write output voltage V_2 as

$$V_2 = \left(\frac{E_m}{1-D} - nV_2 \right) \frac{1}{n} \frac{D}{(1-D)} \quad (18)$$

$$V_2 = \frac{E_m D}{n(1-D)} \quad (19)$$

C. Design of fly back converter.

For Volt second transformer balance

$$(V_1 - V_{sat})D = n(V_2 + V_f)(1-D) \quad (20)$$

At critical inductance L_c , the peak inductor current is twice the average.

$$I_p = 2I_L = \frac{V_{L_2} T_{on}}{L_c} \quad (21)$$

$$I_p = \frac{V_{L_2} D}{f_s L_c} \quad (22)$$

$$I_p f_s L_c = V_{L_2} D \quad (23)$$

we have

$$i_{2(avg)} = \frac{nI_p(1-D)}{2} = \frac{V_2}{R} \quad (24)$$

$$I_p = \frac{2V_2}{R(1-D)n} \quad (25)$$

from (21), (25)

$$L_c = \frac{(V_2 + V_f)R(1-D)^2 n^2}{2V_2 f_s} \quad (26)$$

VII. Design of A 100 Watt, 230 V, 50 Hz, 50 V Dc Single Stage Single Switch Power Factor Converter

A. Calculation of ' L_1 ' using EAC.

Switching instant is considered as $\alpha = 90^\circ$

$$f_s = 20\text{kHz},$$

$$D = 0.26$$

$$P_{out} = V_{rms} \times I_{rms}$$

$$\therefore I_{rms} = \frac{100}{230} = 0.4348\text{A}$$

$$I_m = 0.6148\text{A}$$

Value of I_{peak} is calculated using EAC as follows

$$\frac{1}{2} \times 0.456 \times 50 \times 10^6 I_{peak} = I_m \times \theta$$

$$\frac{1}{2} \times 0.456 \times 50 \times 10^6 I_{peak} = 50 \times 10^6 \times 0.6148 I_{peak} = 2.696\text{A}$$

$$\therefore L_1 = \frac{DTE_m}{I_{peak}} = \frac{0.26 \times 50 \times 10^6 \times 230 \times / 2}{2.696} = 1.57\text{mH}$$

B. Calculation of L_C

L_C is calculated for $D = 0.26$

Using (24), (33) $L_C = 1.2\text{mH}$

C. Calculation of energy storage capacitor.

$$I_{peak} = \frac{DTE_m}{L_1}$$

$$= \frac{0.45 \times 50 \times 10^{-6} \times 230 \times \sqrt{2}}{1.57 \times 10^{-3}}$$

$$= 4.66\text{Amp}$$

$$\text{Energy Stored} = \frac{1}{2} L_1 I^2 = \frac{1}{2} \times 1.57 \times 4.66^2 = 17\text{J}$$

$$\text{Energy Stored} = \frac{1}{2} C_1 V^2$$

$$C_1 V^2 = L_1 I^2$$

$$C_1 \times 540^2 = 1.57 \times 10^{-3} \times 4.66^2$$

$$C_1 = 116\mu\text{F}$$

VIII. Relationship between 'D' and Load

$$\text{We have } I_p = \frac{2V_0}{Rn(1-D)}$$

$$\frac{DTE_m}{L} = \frac{2V_0}{Rn(1-D)}$$

$$V_0 = \frac{Rn(1-D)DTE_m}{2L}$$

$$\frac{EmD}{n(1-D)} = \frac{Rn(1-D)DEm}{2Lf}$$

$$2Lf = Rn^2(1-D)^2$$

$$R = \frac{2Lf}{n^2(1-D)^2}$$

$$n^2(1-D)^2 = \frac{2Lf}{R}$$

$$n(1-D) = \sqrt{\frac{2Lf}{R}}$$

$$1-D = \frac{1}{n} \sqrt{\frac{2Lf}{R}}$$

$$D = 1 - \frac{1}{n} \sqrt{\frac{2Lf}{R}}$$

From the above equation we can conclude that for a given circuit duty ratio is function of load.

IX. Simulation Results.

Simulation of the proposed single stage single switch power factor converter with the designed value of circuit parameters was carried out using Orcad software package. Simulation results were found meeting the design intends.

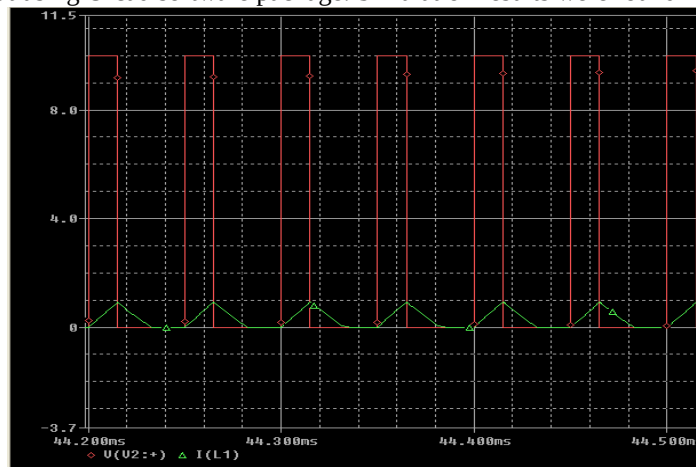


Figure 5: Shows that Input PFC converter works in DCM

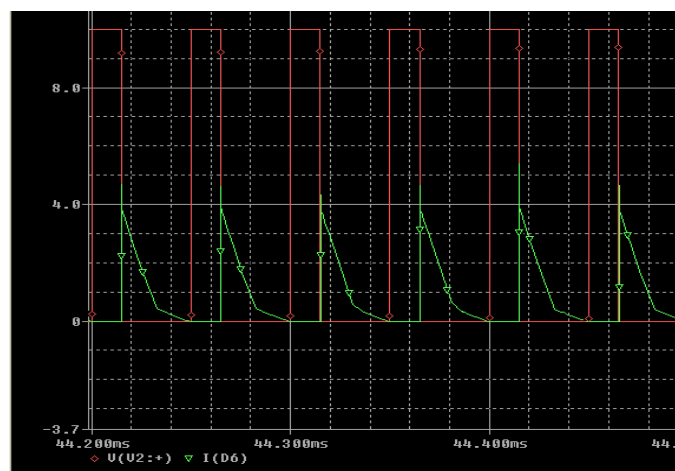


Figure 6: Shows that DC-DC converter operates in CCM

Under closed loop condition when load is suddenly reduced due to the instantaneous power unbalance, the dc bus voltage and output voltage tend to increase. Fig. 7 shows the increase in output voltage is immediately detected by the controller and duty cycle is automatically reduced, the closed loop is found taking the corrective action leading to a new energy balance.

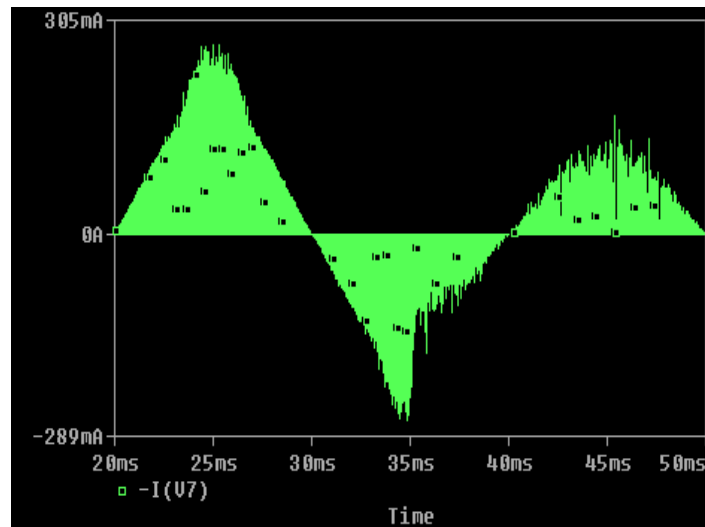


Figure 7: Shows the automatic reduction in the magnitude of input current under closed loop control when the load is reduced after 35ms

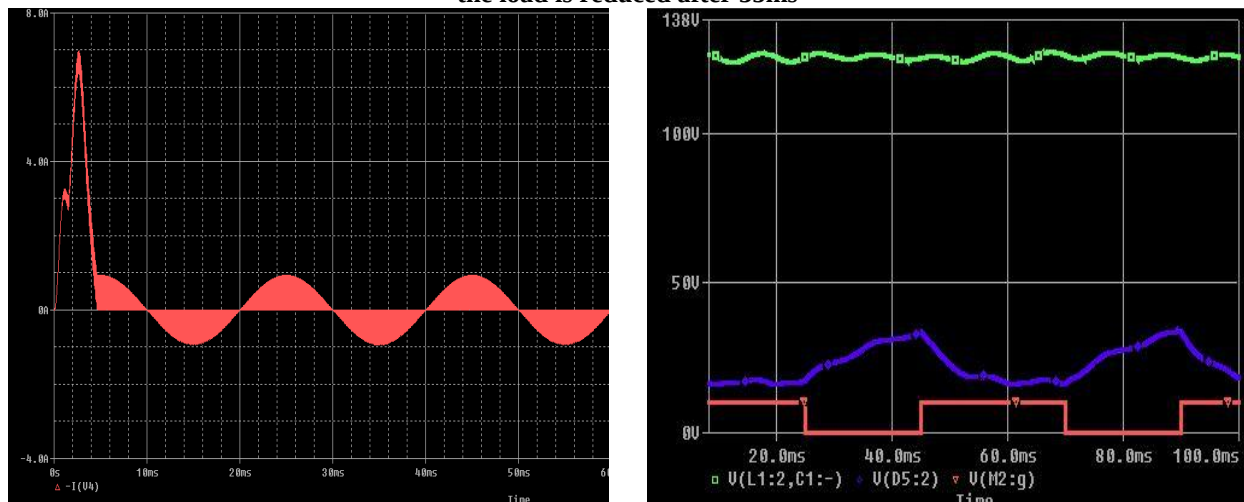


Figure 8: Shows that under open loop there is substantial increase in output voltage when load is reduced after 45 ms also very small changes in the dc bus voltage and no change in input current is seen. Fig. 8 shows under open loop condition input current does not know what happens at the output converter.

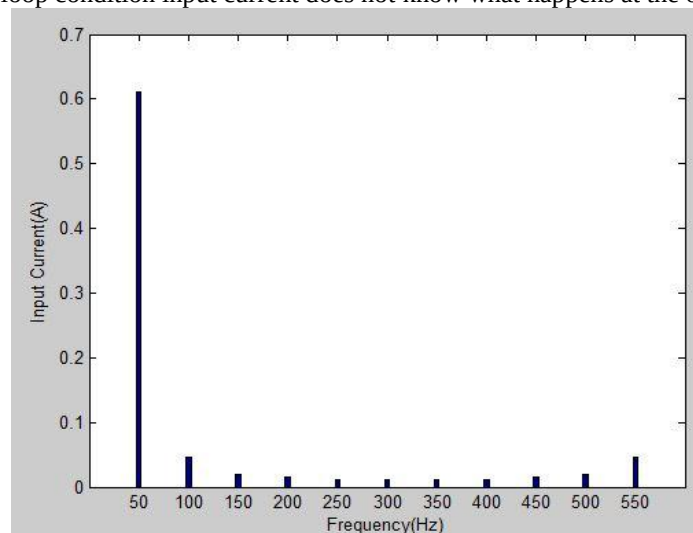


Figure 9: Shows harmonic spectrum of input current in closed loop

Fig.9 indicates fundamental frequency of 50 Hz is dominant and higher order components are insignificant

X. Experimental Results

Experimental 230V, 50Hz input, 10-100V dc, 100w single stage single switch power factor converter has been built and tested using MOSFET IRFPF50 as switch, to verify the results obtained during simulated test. Experimental results are found in line with the results obtained during simulation when tested in open loop as well as closed loop condition. Fig. 10 shows sinusoidal nature of input line current and input power factor close to unity.

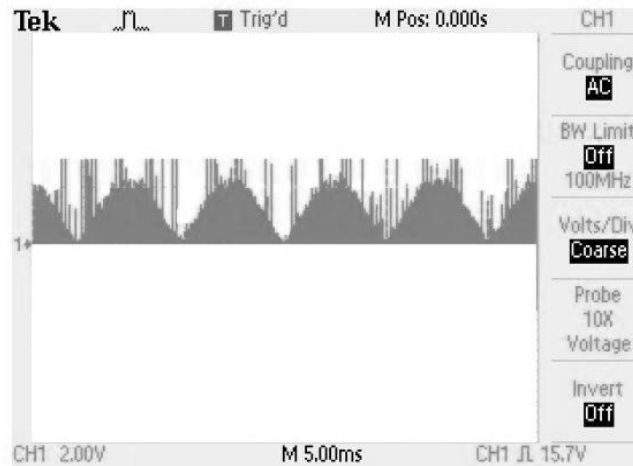


Figure 10: Shows that inductor current drawn is sinusoidal in DCM operation of PFC stage.

XI. Conclusion

Single stage single switch power factor corrected converter design by applying EAC to determine value of boost inductance and by using closed loop control is presented. The dc bus voltage stress at light load is found completely eliminated under closed loop operations. Output voltage regulation using duty ratio variations and fixed switching period is the most simple method of control. For normal performance of the converter the duty ratio needs to be limited up to 0.5. Experimental results demonstrate that it is possible for the proposed converter to have fast response and low line current harmonic content.

XII. References

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