



Optimized Design of High Performance Reversible Multiplier Using BME and MHNG Reversible Gate

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Abstract: Reversible logic circuits are increasingly used in power Minimization having applications such as low power CMOS Design, optical information processing, DNA computing, Bioinformatics, quantum computing and nanotechnology. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. In the present paper an optimized and low quantum cost reversible multiplier using BME and Peres reversible logic gates is proposed. The proposed work is best compared to the other in terms of number of reversible gates and number of garbage outputs.

Keywords: Reversible logic circuit, reversible logic gates, reversible multiplier circuits, quantum computing, nanotechnology based systems.

I. Introduction

Energy dissipation is an important consideration in VLSI design. Reversible logic was first related to energy when Landauer states that information loss due to function irreversibility leads to energy dissipation [1]. Thus reversibility will become an essential property in future circuit design. Reversible logic has applications in various research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and Nanotechnology.

The difference of reversible logic synthesis compared to binary logic synthesis can be summarized as follows [8]:

- 1) The gates used to implement the circuit have the equal number of inputs and outputs.
- 2) Every output of a gate, which is not used in the circuit, is a garbage signal. A good synthesis method minimizes the number of garbage signals.
- 3) The total number of constants at inputs of the gates is kept as low as possible.

However, reversible logic is suffering from two problems. Firstly, there is a lack of technologies with which to build reversible gates. Work is certainly continuing in this area. Secondly, while there is much research into how to design combinational circuits using reversible logic, there is little in the area of sequential reversible logic implementations. There is no limitation inherent to reversible logic preventing the design of sequential circuits; in fact when Tommaso Toffoli first characterized reversible logic in his 1980 work Reversible Computing [4] he stated that "Using invertible logic gates, it is ideally possible to build a sequential computer with zero internal power dissipation." To establish the relevance of reversible and quantum computing it seems appropriate to note that the VLSI industry is moving at high speed towards miniaturization. With miniaturization it faces two issues:

- i) A considerable amount of energy gets dissipated in VLSI circuits and
- ii) The size of the transistors are approaching the quantum limits where tunneling and other quantum phenomena are likely to appear. Thus, we need a superior technology that can circumvent these problems.

This paper is organized as follows: Section 3 gives the brief introduction to some of the important basic reversible logic gates. In Section 4 the proposed design of 2*2 reversible multiplier circuits are explained. Section 5 gives the reversible logic implementation of the proposed designs of multiplier. Section 6 gives the results and discussion and also the comparison of proposed design with other existing circuits. Finally Section 7 concludes with a scope for further research.

II. Reversible Logic

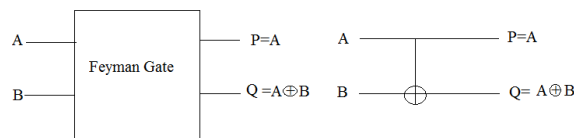
The n -input and k -output Boolean function $f(x_1, x_2, x_3, \dots, x_n)$ (referred to as (n, k) function) is called reversible if :

- 1) The number of outputs is equal to the number of inputs and
- 2) Each input pattern maps to unique output patterns [13]

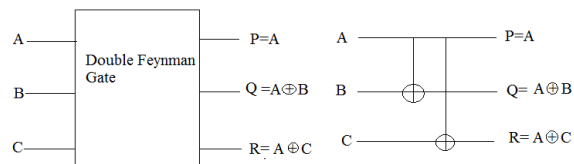
In other words, reversible functions are those that perform permutations of the set of input vectors.

III. Reversible Logic Gates

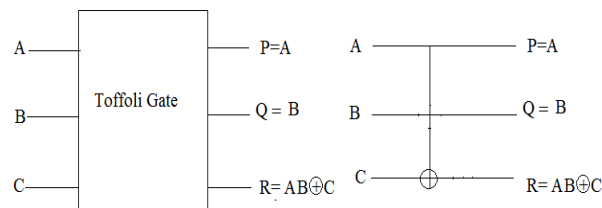
Feynman gate: It is a 2*2 Feynman gate [6]. The input vector is $I(A, B)$ and the output vector is $O(P, Q)$. The outputs are defined by $P=A$, $Q=A \oplus B$. Quantum cost of a Feynman gate is 1.



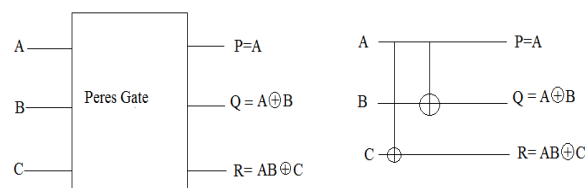
Double Feynman gate: It is a 3*3 Double Feynman gate [6]. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The outputs are defined by $P = A$, $Q=A \oplus B$, $R=A \oplus C$. Quantum cost of double Feynman gate is 2.



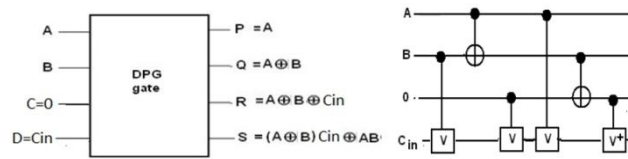
Toffoli gate: It is a 3*3 Toffoli gate [7]. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The outputs are defined by $P=A$, $Q=B$, $R=AB \oplus C$. Quantum cost of a Toffoli gate is 5.



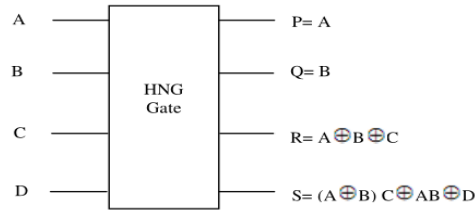
Peres gate : It is a 3*3 Peres gate [11]. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The output is defined by $P = A$, $Q = A \oplus B$ and $R=AB \oplus C$. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.



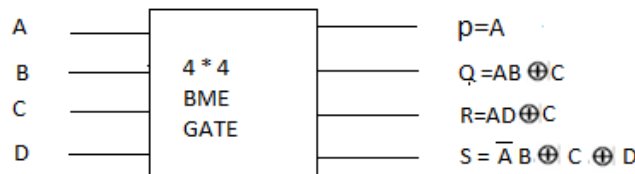
DPG gate: It is a 4*4 DPG gate [25]. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). The quantum cost of DPG gate as full adder is 6.



HNG Gate: It is a HNG Gate[9]. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). $P = A$, $Q = B$, $R = A \oplus B \oplus C$ and $S = (A \oplus B) \oplus C \oplus AB \oplus D$. The full adder using HNG is obtained with $C = Cin$ and $D = 0$.



BME gate : It is a 4*4 reversible logic gate named BME gate[26]. The input vector is I (A,B,C,D) and the output vector is O(P,Q,R,S). The output is defined by $P=A$, $Q=AB \oplus C$, $R=AD \oplus C$ and $S = A'B \oplus C \oplus D$. The Quantum Cost of BME gate is 5.



MHNG gate : It is a MHNG gate[27]. The input vectors is I(A,B,C,D) and the output vectors is O(P,Q,R,S).

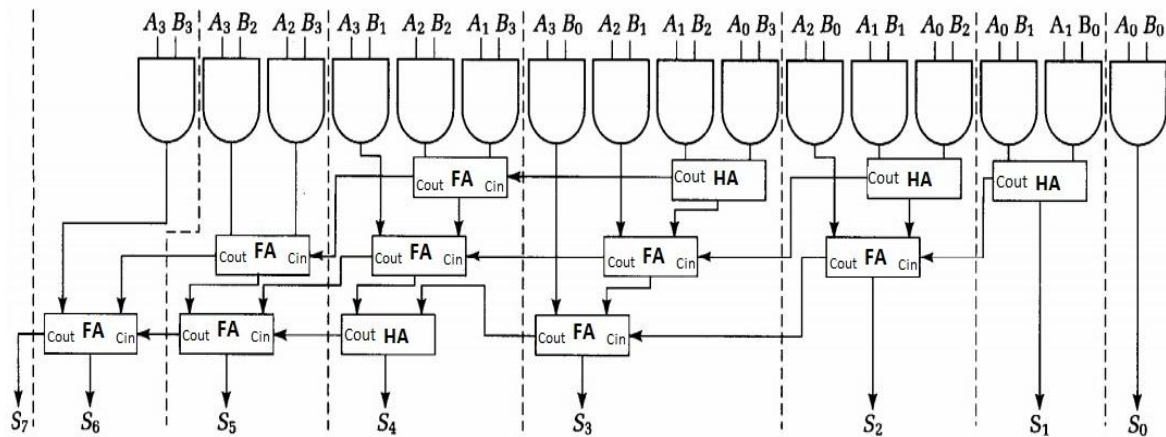


IV. Proposed Reversible Multiplier Circuit using BME, MHNG and Peres reversible gate

The operation of the 4×4 multiplier is depicted fig.11. The block diagram of 4×4 multiplier is shown fig.12. The proposed multiplier has two parts. First, the partial products are generated using BME gate shown in fig.13, then the multi operand addition is performed as shown in fig.14.

$$\begin{array}{r}
 \begin{array}{cccc}
 A_3 & A_2 & A_1 & A_0 \\
 B_3 & B_2 & B_1 & B_0 \\
 \hline
 A_3 \cdot B_0 & A_2 \cdot B_0 & A_1 \cdot B_0 & A_0 \cdot B_0 \\
 A_3 \cdot B_1 & A_2 \cdot B_1 & A_1 \cdot B_1 & A_0 \cdot B_1 \\
 A_3 \cdot B_2 & A_2 \cdot B_2 & A_1 \cdot B_2 & A_0 \cdot B_2 \\
 A_3 \cdot B_3 & A_2 \cdot B_3 & A_1 \cdot B_3 & A_0 \cdot B_3 \\
 \hline
 S_6 & S_5 & S_4 & S_3 & S_2 & S_1 & S_0
 \end{array}
 \end{array}$$

Figure I The block diagram of proposed 4×4 multiplier



V. Partial product generation of proposed Multiplier

Partial products can be generated in parallel using BME gates as shown in Fig13. This uses only 8 BME gates and is a better circuit as it has less hardware complexity and quantum cost compared to other gates [18].

Figure II Partial product generation using BME gate.

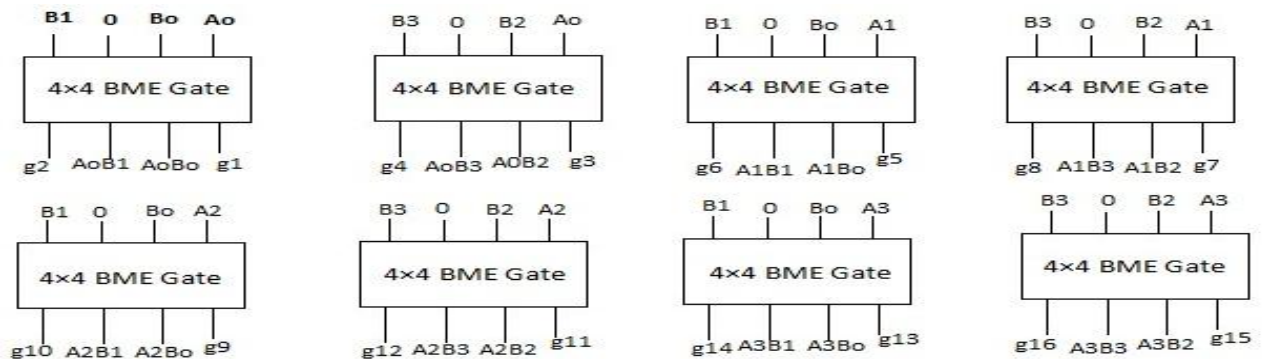
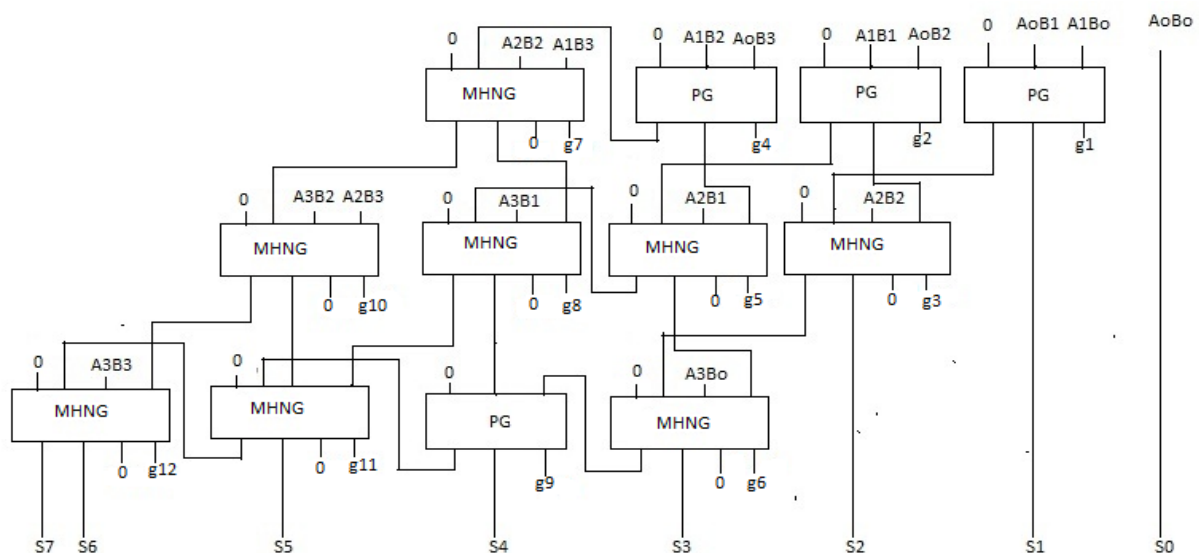


Figure III proposed 4×4 reversible multiplier using PG and MHNG gate.



VI. Result & Discussion

Table-1 gives the comparative study of partial product generation of the circuit and table-2 gives the comparative study of MOA of different designs.

Table I shows the Partial product generation

Partial Product generation	No of gates N	No of Constant inputs CI	No of Garbage outputs GO	Quantum cost QC
Proposed	8	8	16	40
PG[25]	28	40	32	88
MKG[2]	40	40	32	88
PFAG[12]	40	40	32	88
HNG[9]	40	40	32	88
TSG[4]	40	40	32	104

Table-II gives the comparative study of multi-operand addition of the proposed design with other existing designs

Reversible multiplier	No of gates N	No of Constant inputs CI	No of Garbage outputs GO	Quantum cost QC
Proposed	12	12	12	64
PG[25]	12	12	20	64
MKG[2]	12	16	24	120
PFAG[12]	12	12	20	80
HNG[9]	12	12	20	64
TSG[4]	13	18	26	130

Now we prove that the total calculation of partial product generation and multi-operand addition of this proposed 4×4 reversible multiplier is better than other both in garbage output and constant input . And has the minimum quantum cost than using MHNG[20] ,HNG ,MKG ,TSG as respectively [17] show in **table-III**. The comperative results are given bellow

Reversible multiplier	No of gates N	No of Constant inputs CI	No of Garbage outputs GO	Quantum cost QC
Proposed	20	20	28	104
MHNG[27]	28	28	22	Not defined
[24]	28	28	32	Not defined
[23]	28	28	28	Not defined
[22]	28	28	52	Not defined
[21]	28	32	56	Not defined
[20]	29	34	58	Not defined
[19]	40	31	56	Not defined
PG [25]	40	52	52	152
MKG[2]	52	56	56	208
PFAG[12]	52	52	52	184
HNG[9]	52	52	52	152
TSG[4]	53	58	58	234

VII. Conclusion

In this paper, we presented a 4x4 bit reversible multiplier circuit using MHNG gates, BME gates and Peres gates. Table-3 demonstrates that the proposed reversible multiplier circuit is better than the existing designs in terms of hardware complexity, number of logic gates, garbage outputs, constant inputs and optimized in terms of area and delay time. Our proposed reversible multiplier circuit can be applied to the design of complex systems in nanotechnology.

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