



DESIGN OF FAST SWITCHING IGBT GATE DRIVER FOR HIGH RATED MODULES

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Abstract: The past decades Insulated Gate Bipolar Transistors (IGBT) have witnessed the continuous increase in sinusoidal pulse width modulation (SPWM) inverter's switching frequency. For sequential switching of three phase inverters a high frequency isolated fast switching IGBT driver circuit is recommended.. High voltage ratings are attractive for pulsed power and high-voltage switch-mode inverter applications. In this a push-pull converter topology is implemented for 1200V high voltage with 10KHz to 50KHz switching frequency for the IGBT driver circuit. High switching frequency provides fast transient response, small component size and high power density. The present circuit produces low gate drive loss, fast switching speed and has immunity to false trigger IGBT driver circuit function is verified with CRO external results

Keywords: IGBT Gate driver, Push-Pull converter, fast switching speed, 2 level turn OFF.

I. Introduction

The applications of insulated gate bipolar transistors (IGBT's) have expanded widely, particularly in the area of Grid tied voltage source inverters and single phase, three Phase bridge type inverters. The gate drive circuit in the power converter is the interface between the IGBT power switches and the logic-level signals in the modulator. Gate drive circuits for power inverters and converters require electrical isolation. Among various isolation techniques isolation transformer is used here. Because the gate drives circuit can be optimized to achieve the best performance that can be obtained from the power semiconductor device. It operates as a MOSFET with an injecting region on its Drain side to provide for conductivity of the Drain drift region so that on-state losses are reduced. The essential requirements for the Gate drive are

(a) Less delay time for turn-ON and turn-OFF (b) Reduced turn-ON & turn -OFF losses.(c) Reduced to over voltage at turn- OFF

II. Design and analysis Of IGBT Driver

High-voltage (>1200 V) IGBTs are commonly used as modules with ratings from 70 to over 1500 A, aimed at motor control , grid tied inverters and traction applications. Increasing the voltage ratings of IGBTs reduces turn-ON and Turn-OFF di/dt and increases the switching loss. For systems that require higher switching frequencies such as inverters and pulsed power applications fast switching is essential to the optimum performance of the system resulting in reduced Turn-ON and Turn-OFF losses^[1].The switching behavior (turn-on and turn-off) of an IGBT module is determined by its structural internal capacitances(charges) and the internal and external resistances. When calculating the output power requirements for an IGBT driver circuit, the key parameter is the GATE CHARGE. IGBT Capacitances are as shown in figure 1.

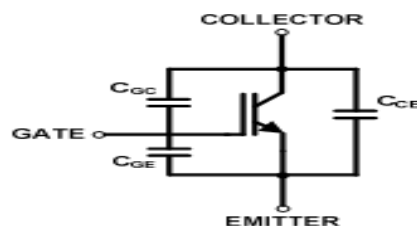


Fig .1: IGBT Capacitances

This gate charge is characterized by the equivalent input capacitances C_{GC} and C_{GE} . In IGBT these capacitances are specified as voltage- dependent low-signal capacitances of IGBT in the "Off" state. The capacitances are independent of temperature , but dependent on the collector-emitter voltage. Low-Signal

Capacitances are referred are $C_{ies} = C_{GE} + C_{GC} =$ Input capacitance, $C_{res} = C_{GC} =$ Reverse transfer capacitance, $C_{oes} = C_{GC} + C_{CE} =$ Output capacitance The drive peak current value I_{GP} can be approximately calculated as

$$I_{GP} = \frac{(+V_{G(ON)} + |-V_{G(OFF)}|)}{R_G + R_g} \quad \dots\dots\dots(1)$$

+ $V_{G(ON)}$ = forward bias supply voltage 15 V, $-V_{G(OFF)}$ = Reverse bias supply voltage -5V, R_G = Drive circuit Gate Resistance = 2 Ω R_g = Modules internal resistance. Input capacitance $C_{ies} = 13nF$. For 1200V/70A U-series IGBT module and $I_{GP} = .87A$. The gate charge is the basic parameter used to determine driver output power and gate current^[2]. The gate charge current $Q_G = 2.15\mu C$. The real gate charge $Q_{1G} = 0.8 * Q_G$ for (-5V/ 15 V). Electrical energy(E) required for driver is

$$E = Q_{1G} * (V_{G(ON)} + |-V_{G(OFF)}|) * F_{sw} \quad \dots\dots\dots(2)$$

$E = 0.06Wt$, Average, Gate current $I_G = Q_G * F_s = 0.5 A$

A. Voltage Source Inverter with IGBT

A typical three phase voltage source bridge type inverter circuit diagram is shown in figure.2. Single-phase control method was expanded in a three-phase inverter bridge by duplicating three individual phases with 120° apart. For each phase one IGBT driver circuit is designed duplicating three individual phases with 120° apart. For each phase one IGBT driver circuit is designed. In each phase for positive and negative side of the IGBT triggering delay is provided to reduce over lapping in positive and negative side. Grid tied inverters are widely used in solar power generation, which converts generated DC into AC at online solar grid applications. The layout of IGBT driver circuit module at testing is as shown in Fig 3.

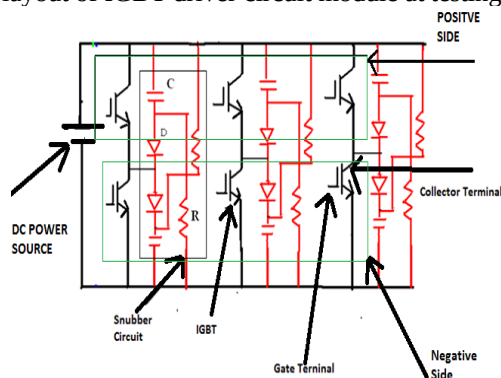


Fig:2 Three phase inverter



Fig 3: IGBT driver circuit layout

III GBT driver circuit

Fig 4 shows the circuit diagram of IGBT gate driver circuit. Gate driver circuit design is the prominent issue of the inverter design because to achieve the fast switching response of the high rating IGBT switches. The PWM output pulses, 1MHz square pulses are given to the AND gate. It compares the two inputs and the output given to the MOSFETs to drive push-pull transformer. push-pull converter provides isolation for the gate driver circuit. Push-Pull converter output is fed to IGBT gate terminal through driver circuit.

Under short circuit conditions gate voltage surges will cause gradation of short circuit withstanding capability by allowing higher than normal currents to flow. In order to control gate voltage surges it is often desirable to implement gate voltage clamping on the gate side of the series gate resistor R_g . For gate voltage clamping zener diodes Z_1 and Z_2 are connected from gate to emitter as shown in figure 3. In order for the gate voltage clamping circuit to be effective it must be connected as close as possible to the gate and emitter terminals IGBT module. For 15V gate drive 16V to 18V zeners are used^[3]. Negative gate voltage -5V during turn-Off process can be obtained from D_3 and D_4 diodes which are connected to push-pull transformer output. this negative voltage is used in two level Turn-off process. The delay is provided with R_0 and C_0 , SPWM output pulses are given through delay circuit to positive and negative side firing of the dual IGBTs. This delay prevents false turn-ON of positive and negative triggering IGBTs.

A. Turn ON process

In order to establish collector to emitter conduction in an IGBT module a positive voltage must be applied to the gate. A gate voltage of 10V would be sufficient to fully turn the device on but it may not be

sufficient to obtain efficient switching. If 10 volts were used for V_{ON} a long dynamic saturation (slow turn-on) will result because the gate voltage takes a long time to reach 10V as it exponentially charges through the series gate resistance. For optimum performance a turn-on gate voltage of $15V \pm 10\%$.

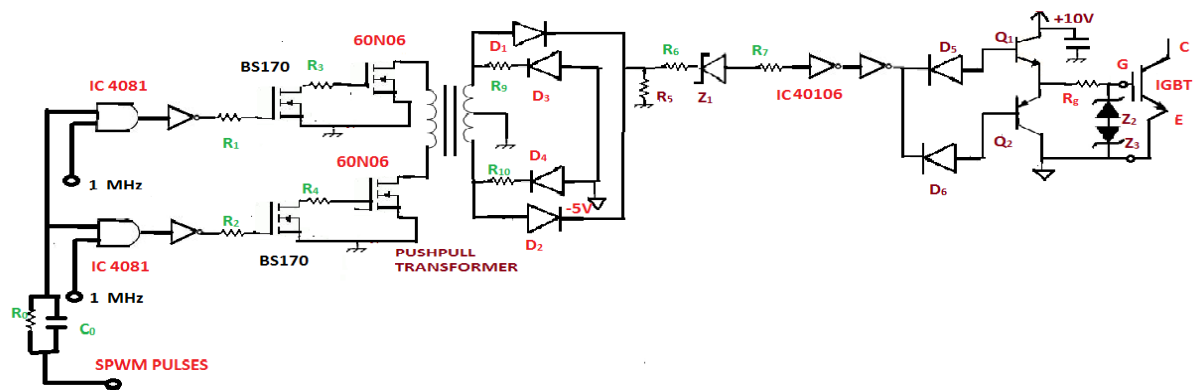


Fig 4: IGBT driver circuit diagram

Using a voltage in this range will ensure that the device stays fully saturated and switches on efficiently while maintaining good short circuit durability. The absolute maximum voltage is $15V \pm 10\%$. Application of voltages greater than 15V may cause breakdown of the gate oxide resulting in permanent damage to the device. The 15V upper limit must be restricted even further if short ^[4] circuit survival is required. The short circuit withstand time (t_w) of a given device is inversely proportional to the product of applied voltage and short circuit current. The short circuit current increases with increasing gate voltage thus degrading the withstand time.

B.Designing of Push Pull Converter

A push-pull converter is a type of DC to DC converter that uses a transformer to change the voltage of a DC power supply. The transformer's ratio is arbitrary but fixed. push-pull topology refers to a two-switch topology with a split primary winding. push pull converter circuit operation is as shown in fig 5. The push-pull topology is basically a forward converter with two primaries. The primary switches alternately power their respective windings. When switch TR_1 is turned ON, V_s is applied to lower half of transformer primary $V_1 = V_s$. As a result voltage $V_2 = (V_s / N_1) * N_2$ is induced in both secondary windings. Voltage in the upper half secondary forward bias diode D_2 therefore the output voltage V_o is given $V_o = (V_s / N_1) * N_2$. When TR_2 switch is turned on, $V_1 = -V_s$ is applied to upper half of primary winding. Consequently, $V_2 = -(V_s / N_1) * N_2$ is induced in both transformer secondary's. As V_2 is negative then diode D_1 gets forward biased. As for the dot notation current flows through D_2 . when switch TR_2 is active as for the dot notation current flows through D_1 . D_1 and D_2 switching wave forms are as shown in fig 5. Push pull converter output is shown in fig 6. Power $P_{O2} = (V_o + V_s)I_o$. Substituting the values for the variables we have $P_{O2} = 15.15$ watts.

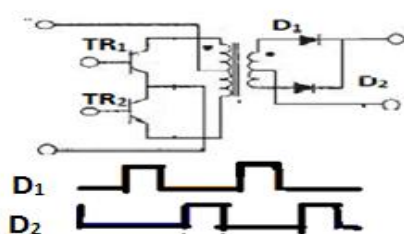


Fig 5 : Push Pull Converter Circuit Operation Fig



Fig 6 : Push Pull Converter output

The area product for this converter configuration is given below by equation 3. Where A_p = area product of converter, A_c = core cross section area, A_w = window area Suitable Values for the variables we have $A_p = 2.9 * 10^{(-8)} m^4$, and the sufficient core of ferrite core is P 30/19 is a proper choice $A_c = 130 mm^2$, $A_w = 747 mm^2$.

$$A_p = \frac{\sqrt{2} P_{O2} (1 + \dots)}{4 K_m B_m} \dots \dots \dots (3)$$

IV Turn off Process Of IGBT

A substantial off bias of at least -5V is recommended for large IGBT modules. Use of an off bias voltage will reduce turn-off losses and provide additional dV/dt noise immune. Large IGBT modules generally require a stronger off bias than other power MOS devices for two reasons. First, IGBTs typically operate at higher voltages resulting in increased dV/dt coupling of switching noise. Secondly, large IGBT modules that are constructed from parallel chips have internal gate resistors in series with each chip.

A. Two level turn off function

Short circuit over current in the load, large overshoot can occur across IGBT at turn-off and can exceed IGBT breakdown voltage. By reducing the gate voltage for a short time before turn-off, the IGBT current is limited and potential over voltage is reduced. This technique is called 2 level turn off. This can be achieved by provide negative bias during turn-OFF IGBT.

B. Technique to generate negative bias during turn-OFF

Importance of negative bias during turn-off to quickly remove any charge on the C_{GS} and C_{GD} . In the case of IGBTs, this considerably accelerating turn-off. The turn-ON speed of a IGBT can be increased only up to a level matched by the reverse recovery of rectifiers or diodes in a power supply, because in an inductive clamped load, turn-ON of a IGBT coincides with turnoff (or reverse recovery completion) of the rectifier diode. Too fast a turn on could also cause oscillation in the Drain or Collector current. However, it is always beneficial to have a driver with intrinsic low turn-on time a series gate resistor.

The collector voltage rise during turn-OFF circuit of the IGBT causes the gate voltage to charge up because of the displacement current through the gate-collector capacitor. The gate voltage goes above the threshold voltage, which results in excess carriers being injected into the IGBTs' buffer region through the gate channel. This results in a lower turnoff and a reduced overvoltage during turn-off. The gate is discharged slowly during turn-off operation. This process continues through the rising period of the collector voltage and the falling period of the collector current. After that the gate voltages rapidly attain its final negative value. The total switching time is also reduced. Any re-turn-on of the IGBT is prevented in because the gate current remains negative during turn-off., thus ensuring stable operation. To provide a negative gate bias of -5V by D_3 and D_4 . This ensures adequate turn-off for the application and to negate the effect of Miller induced current in a bridge configuration if a high dV/dt is applied to the devices. This circuit uses a transformer to provide isolation for the gate drive power supply,. The IGBT's Gate-Emitter voltage now swings from -5V to 15V during the switching transition.

C. Gate driver state operation

A totem pole is a certain type of driver, used to amplify square waves into stronger square wave for driving other types of semiconductors faster. A totem pole consists of a PNP and NPN transistors arranged emitter to emitter, with their bases coupled together. The output signal is taken from where the emitter of the NPN transistor and collector of the PNP transistor meet. A totem pole driver can be used to more effectively drive MOSFETS and IGBT'S. It increases the strength of the gate signal and improves stability of gate drive. The amplified gate current allows the semiconductors to turn-ON and turn-OFF with faster speed. The Circuit diagram of a gate driver is depicted in Fig 7. The driver consist of gate resistors of Turn-ON resistor R_{G-ON} and Turn-OFF resistor R_{G-OFF} . Turn-ON R_{GON} and turn-OFF resistor R_{G-OFF} are fed to IGBT gate terminal. Low impedance output amplifier composed of transistors Q_1 and Q_2 . A control unit that is a Push-Pull converter drives those transistors Q_1 and Q_2 . The gate driver power supply V_{CC} is (15V) and V_{EE} (-5 to -15 V). The gate resistors are utilized to limit the gate current and adjust commutation dynamics of the IGBT. At the moment t_0 , the transistor Q_2 turns on. The input gate capacitance C_{GE1} is charged by the positive supply voltage through the resistor R_{G-ON} . The gate emitter voltage V_{GE1} increases from the initial negative voltage V_{EE} toward the positive gate supply voltage V_{CC} .

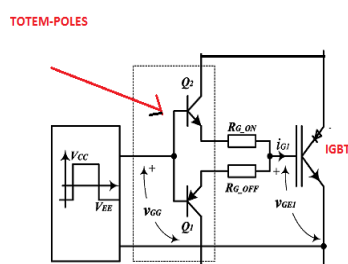


Fig 7: Gate driver state circuit diagram Fig

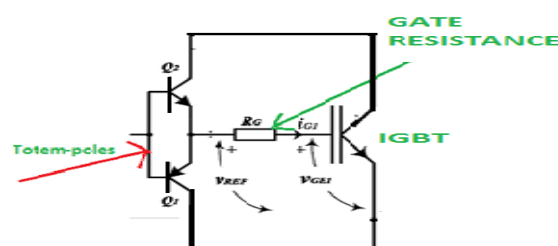


Fig 8: Quasi-steady-state model

To compute the collector current slope quasi-steady-state will be used. Quasi-steady-state equivalent circuit diagram of Fig 8 and the voltage designated as V_{GE1} is voltage across the gate emitter connection on the chip. In a real IGBT module; however, there is a parasitic inductance L_{E1} between the auxiliary emitter and the emitter connection on the chip level, is shown in Fig 8. The gate resistor is normally selected for the tradeoff between reverse recovery current and turn-ON losses.

The gate resistor is normally selected for the tradeoff between reverse recovery current and turn-ON losses. The IGBT gate driver output is as shown in Fig 9. The IGBT output wave having the frequency 20kHz and this frequency depends on sinusoidal pulse width modulation frequency^[5-6].

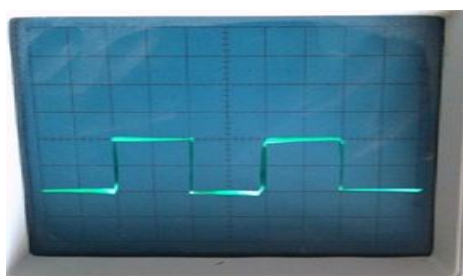


Fig 9: IGBT driver circuit output Fig



Fig 10: IGBT driver circuit output for single phase

Positive and Negative side of the bridge type dual IGBT output is as shown in Fig 10. Positive and negative gate pulses are provided with delay to prevent the device from short circuit at triggering of IGBT gate.

V Conclusion

The novel push-pull converter topology is implemented on PCB board with fast switching and results 1200V IGBT. IGBT driver circuit produces low gate drive loss, fast switching speed and has immunity to false trigger. Two-level turn-off driver reduced turn-off and to present a solution when the IGBT goes out-side the safe operating area at both turn-on and turn-off. The advanced functions of stable operation and false turn-on protection proposed inside this integrated circuit allow safe and reliable operation, with a minimum of external components, in applications such as motor control and single phase, 3 phase bridge circuits.

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