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Design of Adder logic cell with XOR gate

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Abstract: *Adder logic cell is basically an important part of adder sub-system and is well known by the designers so many researchers are still working in this field for speeding up the circuit process along with power consumption. These cells are used in various application as DSP, microprocessors etc. In today's modern world Complementary Metal Oxide Semiconductor (CMOS) design techniques are used for designing so that power, area, delay may be reduced. In this paper designing of Adder Logic Cell is done with the help of XOR/XNOR gate using Microwind software. Here 120nm and 70nm technology is used.*

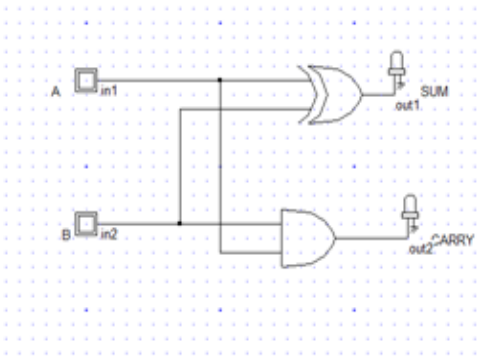
Keywords: *Adders, Area, CMOS Design, Low power*

I. Introduction

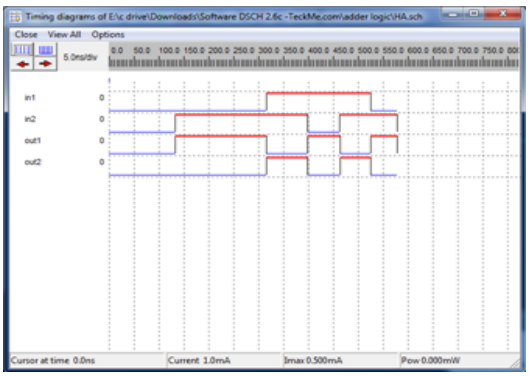
According to Moore's law "The number of transistors double once in every eighteen months" which indicates that many transistors are used being integrated to perform function of device thus huge amount of power is being dissipated. This cause a major problems for the designers hence from there researchers are investigating on this part : how the circuit can be modified so that power consumption can be reduced , some techniques being developed for that as leakage power reduction, reduce number of transistors etc. So while designing of Adder Logic Cell same thing is considered that is power consumption, area captured be less, or processing speed be fast. Adder plays a very important role in digital arithmetic as many sub system like multipliers are designed using it so while designing of Adder Logic Cell (a sub-part of adder) XOR gate is used as it is very efficient.
In this paper designing is done under Microwind software and XOR gates are designed using 3, 4 & 6T (transistor) shown in figure 2(a-c). Each schematic designing is done under DSCH (a sub part of Microwind) tool with 120nm technology and with respect to that simulation are performed under Microwind with 70nm technology.

II. Adder Schematic Design with XOR/XNOR gate

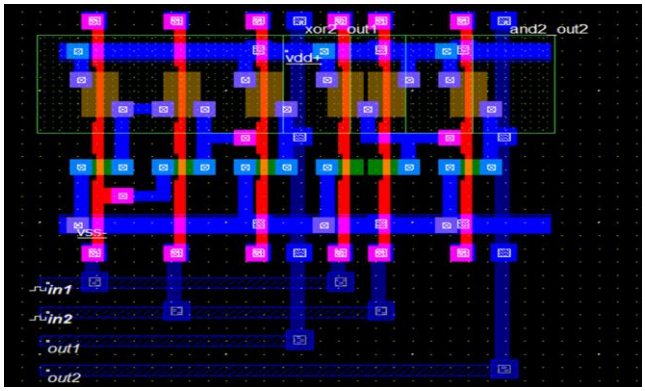
As in digital arithmetic system for performing basic mathematical and comparative operation controller needs an ALU (Arithmetic Logical Unit) and Adder is an important part of this ALU. So here an efficient Adder (Adder logic cell) is designed which dissipates less power. Fist a conventional Half Adder is implemented with two inputs say A, B and Sum, Carry as output shown in figure 1(a) and then this Half Adder is implemented with XOR gates shown in figure 3(a-c) its layout diagram shown in figure 4(a-c) And its simulation is shown in figure 5(a-c) which done by Microwind tool.



(a)

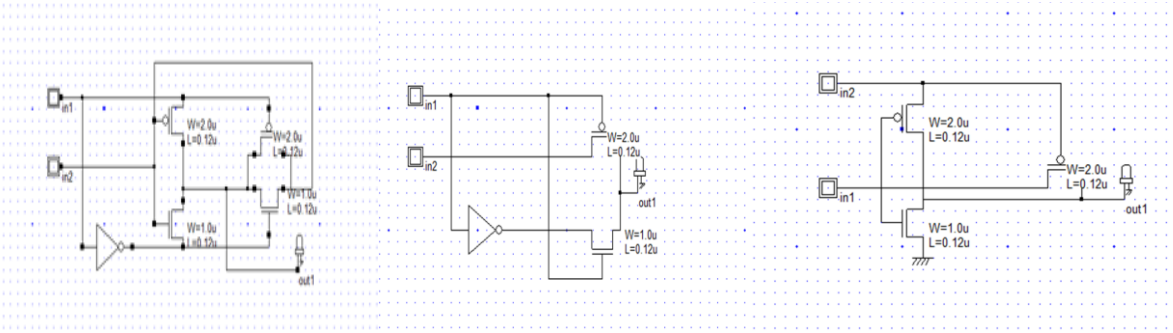


(b)



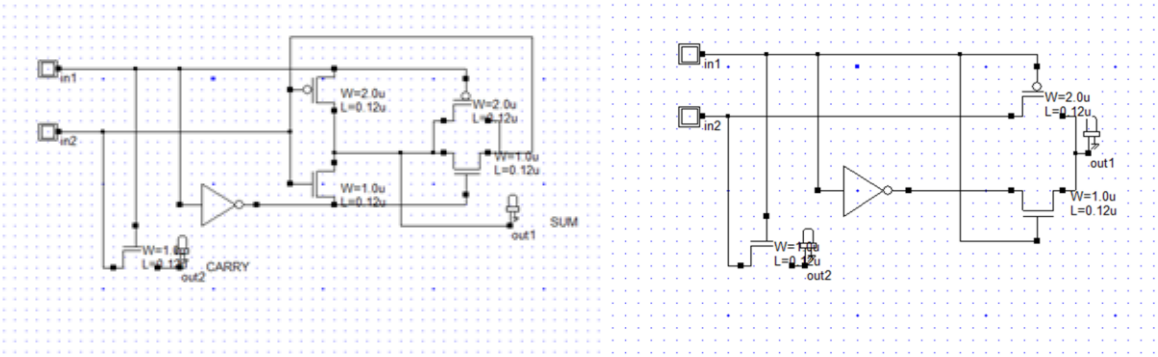
(c)

Figure 1(a-c): (a) Conventional logic diagram (b) Timing waveform & (c) Layout diagram of Half adder

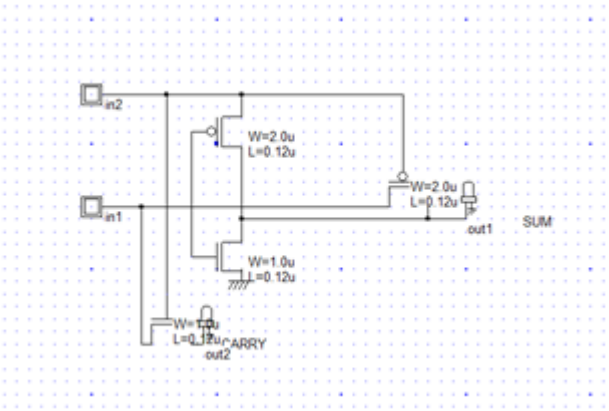


(a) **(b)** **(c)**

Figure 2 (a-c): XOR gate with (a) 6T (b) 4T & (c) 3T

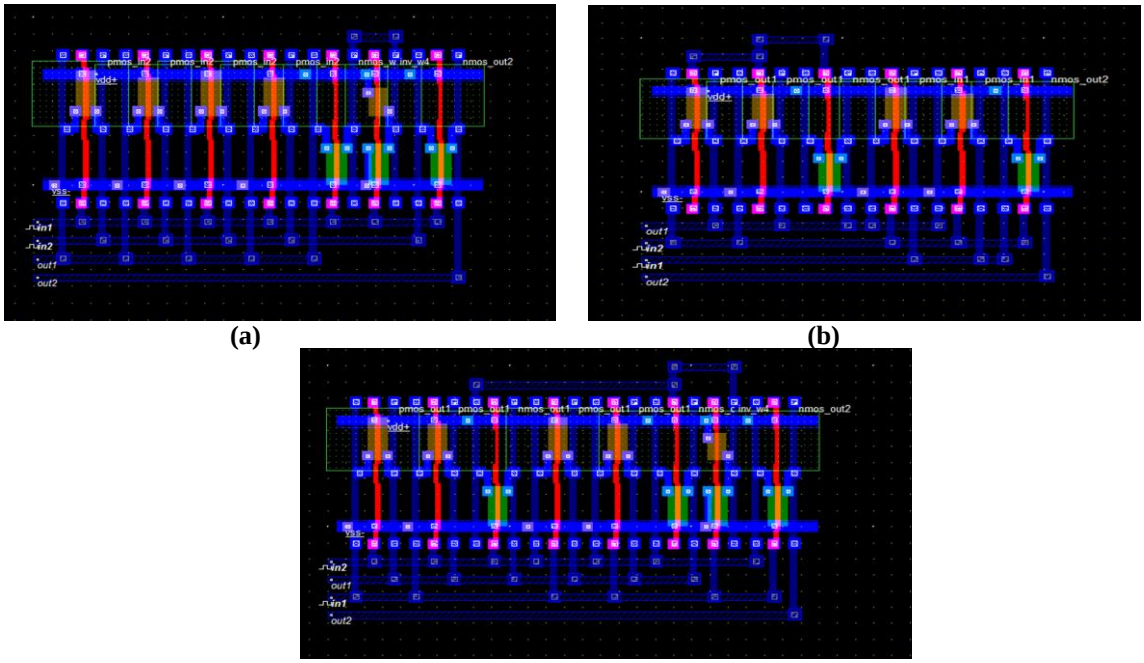


(a) **(b)**



(c)

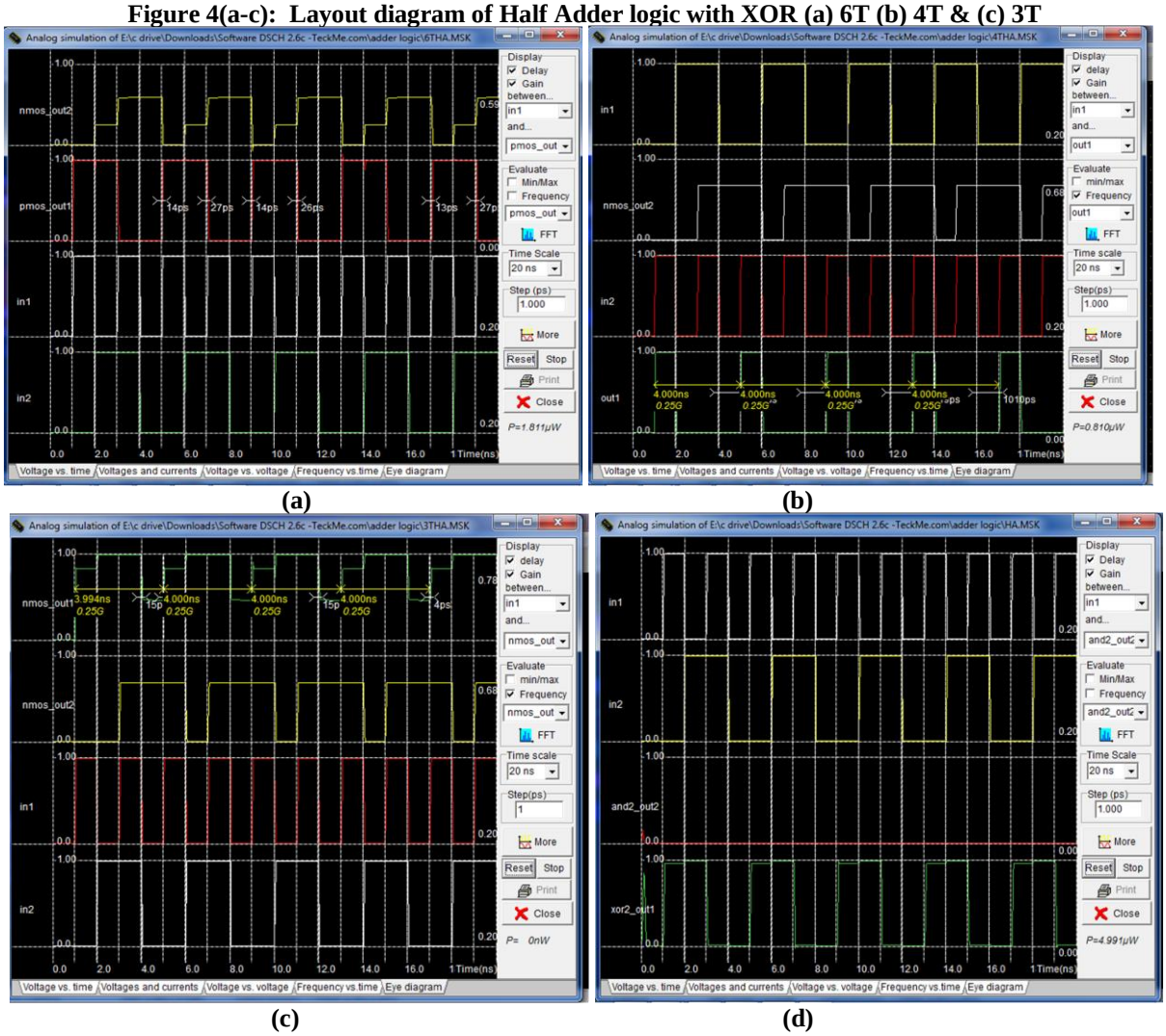
Figure 3(a-c): Half Adder logic with XOR (a) 6T (b) 4T & (c) 3T



(a) **(b)**

(c)

Figure 4(a-c): Layout diagram of Half Adder logic with XOR (a) 6T (b) 4T & (c) 3T



(a) **(b)**

(c) **(d)**

Figure 5(a-c): Simulation result of Half Adder logic with XOR (a) 6T (b) 4T (c) 3T & (d) Conventional

III. Result and Discussionion

All results obtained by simulation is shown in table below and found that for low power 3T XOR gate design can be considered but area wise other design to be considered. Based on table a graphical analysis of power and area is shown.

Table I: Simulation results on layout of Adder logic cells

Design Styles	Power (µW)	Layout Area(µm^2)	Transistors count	Routed wire numbers
Conventional	4.991	30.9	12	6
6T XOR	1.811	69.8	7	22
4T XOR	0.810	47.1	5	13
3T XOR	Very low (nW)	55.6	4	16

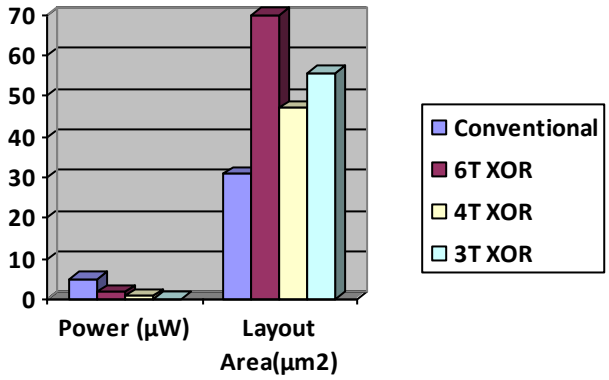


Figure 6: Graphical presentation of Simulation result obtained on power and area

IV. Conclusion

Adders as said an important part of ALU & has biggest role in operation like filtering, signal processing, multiplication etc. In short works as foundation for big system designs. Here XOR/XNOR gate is used for design implementation which reduces power due less number transistors used as shown in table 1 but area wise other is better. Hence this work can be implemented in other fast adder sub system such Look Ahead Carry Adders, Ripple Carry Adder, Multipliers etc. for better performances.

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