International Journal of Engineering, Business and Enterprise Applications (IJEBEA)

www.iasir.net

Timing Jitter and Quantization Error Effects on the performance of Sigma Delta ADC used in SDR Receivers

Preeti Trivedi[1], Dr. Ajay Verma[2]
[1]Assistant Professor, SGSITS, Indore, Madhya Pradesh, INDIA
[2]Prof. and Head, IET, DAVV, Indore, Madhya Pradesh, INDIA

_____

Abstract: This paper presents the effect of timing jitters on the performance of sigma delta ADC for SDR mobile receivers. The time-varying behavior is caused by the non-stationary nature of the clock jitter process. Jitter is the limiting effect for high speed analog to digital converter with high resolution and wide digitization bandwidth, which are required in receivers in order to support high data rates. Mathematical modeling has been done for the same to show the effect of clock jitter as well as aperture jitter on the performance of Sigma delta ADC for SDR mobile receivers in terms SNR. The present work shows that there is degradation in the system performance due to timing jitters. It is also shown that when clock jitter becomes more dominant, increasing the OSR does not improve the performance of Sigma Delta ADC. SNR with quantization error (SQNR) has been evaluated using second order sigma delta ADC. It is shown that at 256 OSR the SQNR is 118.9dB which is very close to the calculated theoretical value. Simulation has been done using SD toolbox of MATLAB Simulink.

Key Words: Sigma delta ADC, Clock jitter, Aperture jitter, Software Defined radio, Signal To noise ratio (SNR).

_____

I.   Introduction

A radio that defines in software its modulation, error correction and encryption processes, exhibits some control over the RF hardware, and can be reprogrammed is clearly Software radio [2]. The wideband ADC is one of the most challenging tasks in software radio design. The input analog signal is sampled at a frequency f_s, which converts it into a discrete time signal. The rapid development of digital wireless system has led to a need for high resolution and high speed band pass analog to digital converters. Continuous time band pass Sigma delta modulator are very suitable for such high frequency application.

To achieve high-resolution without requiring high precision analog components, over sampling techniques are often used. This relies on three techniques: oversampling of the input signal, quantization error shaping and digital filtering. The core circuit of the ADC is a sigma-delta modulator, which acts as a high pass filter to filter the quantization error in the signal bandwidth. Because of the over sampling that makes the signal bandwidth much smaller than half of the sampling frequency, a digital decimation filter can be used to down sample and filter the modulated signal to the Nyquist bandwidth. In Sigma–Delta Modulators, the over sampling is used along with noise shaping to get rid of the quantization error as much as possible. By introducing a Digital to analog filter in the feedback loop, thereby feeding back the quantized signal back to the input as depicted in Figure 1, the shape the quantization error can be out of band of interest[1-3].

The paper is organized as follows: The timing jitters are introduced in section III. An. Jitter model is discussed in sectionIV. SNR calculation is given in section V, Results are discussed in section VI and the work is concluded in section VII.

The present work presents a technique called oversampling technique to reduce the timing jitter effects using oversampling method.

II.   Timing Jitters

The rapid development of digital wireless system has led to a need of high resolution and high speed analog to digital converter. The performance of a data converter is dependent upon the accuracy and stability of the clock supplied to the circuits. When data converter employs a high sampling rate, clocking issues become magnified and significant distortion can be result[13].

Analysis of Signal to noise ratio

For a sinusoidal signal which does not exceed the FSR of the ADC, the SNR due to the quantization error is given by

$$SQNR = 6.02N + 1.76 + 10log_{10}\left(\frac{f_s}{2f_c}\right)dB \qquad (1)$$

Here f_s is the sampling rate and f_c is the maximum frequency of analog signals and N stands for bit resolution and also given by

$$SQNR = 6.02N + 1.76 + 10log_{10}(k)dB \qquad (2)$$

_____

Where $k = f_s/2f_c$.

For sampling rate equal to the Nyquist rate (k=1) then
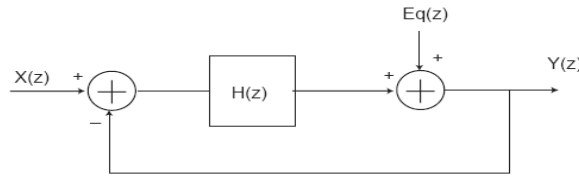
$$SQNR = 6.02N + 1.76 \tag{3}$$

Figure 1. Signal Flow of the Sigma-Delta Modulator

It is seen that the signal transfer function is simply a delay, while the noise transfer function is a discrete-time differentiator. Analysis of the first-order sigma-delta modulator reveals that the quantization noise power is given by (4).

$$P_q = \frac{V_{LSB}^2 \pi^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{4}$$

Where V_{LSB} amplitude of signal and OSR is is oversampling ratio defined as the ratio of f_s to nyquist frequency $2f_c$. So the SNR of the sigma-delta ADC with first order noise shaping is

$$SNR = 20log_{10}\left(\frac{P_S}{P_e}\right)$$

$$SNR = 10log_{10}\left(\frac{3}{2}2^{2N}\right) + 10log_{10}\left(\frac{3}{\pi^2}OSR^3\right) \tag{5}$$

For improving the SNR, increase the OSR. In second-order modulator, the improvement is 15dB with doubling the OSR while for the first-order modulator the improvement is only 9 dB. SNR for m^{th} modulator is given by

$$SNR = 20log_{10}\left[(2^n - 1)\sqrt{3/2}\frac{\sqrt{2m+1}}{\pi^m} OSR^{(m+1/2)}\right] \tag{6}$$

Here m is the order of filter, OSR is the oversampling ratio. The SNR can be calculated using various loop orders (m= 2, 6, 8) and 1-bit quantizer (n=1). With varying the OSR, different gains in SNR can be achieved.

III.   Jitter Model in High Speed ADC

In circuit design that involves the use of a high-performance, high-speed analog-to digital converter (ADC), one of the main care is the clocking scheme. The conversion process starts when a clock signal tells the Sample and Hold (S&H) to take the samples. Up to that instant, the internal switch on the S&H circuit is closed, allowing the voltage across the capacitor to track the input signal. One of the edges of the input clock then indicates when to open this switch, and the capacitor holds the voltage at that instant in time. A mathematical estimation of the best-case signal-to -noise ratio without other noise sources is

$$\sigma_{jitter}^2 = \frac{1}{T}\int_0^\tau (slope(\tau) X jitter)d\tau = \frac{1}{T}\int_0^\tau \left[\frac{\left(Asin\frac{2\pi\tau}{T}\right)}{d\tau}jitter\right]^2 d\tau \tag{7}$$

$$= \frac{1}{T}Jitter^2\int_0^T\left(\frac{2\pi A\cos\frac{2\pi\tau}{T}}{T}\right)^2 d\tau => \left\langle a = \frac{2\pi\tau}{T}, \frac{da}{d\tau} = \frac{2\pi}{T}\right\rangle$$

$$= \frac{1}{T}\left(\frac{2\pi A}{T}\right)^2 jitter^2 \frac{1}{T}\int_0^{2\pi}(cos^2 a)da \quad = \frac{T}{2\pi}\left(\frac{2\pi A}{T}\right)^2 jitter^2 \left(\frac{1}{T}X\frac{1}{2}(a + sina \times Cosa)\right) \tag{8}$$

$$= \frac{T}{2\pi}\left(\frac{2\pi A}{T}\right)^2 jitter^2 \frac{1}{T}\pi = \frac{1}{2}\left(\frac{2\pi A}{T}\right)^2 jitter^2 \tag{9}$$

The theoretical limitation of the SNR due to jitter is given by

$$SNR(dB) = \frac{S}{N} = 10log_{10}\left[\frac{A^2/2}{\frac{1}{2}\left(\frac{(2\pi A)}{T}\right)^2 Jitter^2}\right] = -20log_{10}(2\pi f_{in}jitter) \tag{10}$$

Assuming all these sources of noise are uncorrelated, the total noise is the addition of a noise term independent of input frequency and a noise term dependent on input frequency [6-7].

The theoretical limitation of the SNR due to jitter and other sources of noise are considered   given by

$$SNR(dB) = 10log_{10}\left[\frac{A^2/\sqrt{2}}{Thermal+Quantization+\frac{1}{2}\left(\frac{(2\pi A)}{T}\right)^2 jitter^2}\right] \tag{11}$$

Two of the most significant timing issues are Aperture Jitter and Clock Jitter, which are produced from timing errors in the sample and hold circuit of an ADC and the decoder circuit of the DAC [1].

 -Aperture jitter-Due to uncertainty in sampled pulse

 -Clock jitter –Due to time variation in clock time period

In [10] Walden discovered the aperture jitter as dominating error effect that limits the achievable SNR. In the last few years different authors derived formulas to quantify the SNR limiting effect of jitter in ADCs. Koyabashi et al. presented a formula which allows to calculate the SNR in the presence of an aperture jitter [13]. The effect of clock jitter was investigated by Awad[7].

A.   Aperture Jitter

In communication system, aperture jitter causes uncertainty in phase of the sampled signal, degradation of the noise floor of a data converter, Aperture jitter is random variation in time of the exact sampling instant that causes phase modulation. It results in an additional noise component in the sampled signal. Aperture jitter is caused both by the sampling circuit and sampling clock, the latter source being closely related to the phase noise of the sampling clock oscillator.

B.   Clock Jitter

Clock jitter is what engineers would readily call time-domain distortion. Clock Jitter is caused by phase noise. The resolution of ADCs with a digitization Bandwidth between 1MHz and 1 GHz is limited by jitter. Clock jitter does not actually change the physical content of the information being transmitted. Depending on circumstance, this may or may not affect the ultimate decoded output [2].
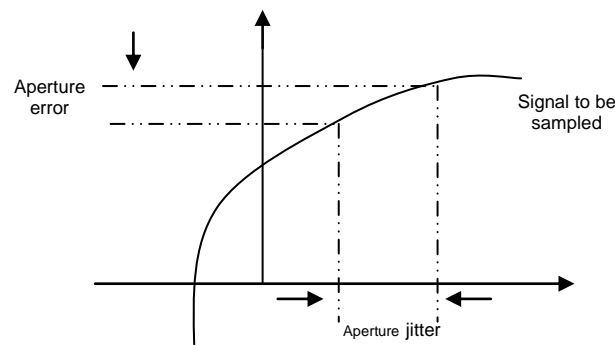

Figure 2: Aperture Uncertainty and Aperture Jitter [2]

C.   Improving SNR by Over Sampling Method

Over sampling is a popular method used for improving SNR in ADC. The input is sampled at a rate higher than the minimum required Nyquist sampling rate, f_s. When over sampling with a factor of k = 16, the same 100-Hz input signal is sampled at 3200Hz. The samples obtained by over sampling are low-pass filtered and decimated using a digital filter to achieve a reduction of the quantization noise. The signal at the frequency band of interest is not affected by the filter, and the result is an improved SNR [13-14].

D.   Aperture Jitter Effect in Sigma Delta ADC

Aperture jitter is random variation in time of the exact sampling instant that causes phase modulation and results in an additional noise component in the sampled signal. Aperture jitter is caused both by the sampling circuit and sampling clock, the later source being closely related to the phase noise of the sampling clock oscillator. In communication system, aperture jitter causes uncertainty in phase of the sampled signal and degrades the noise floor of a data converter. Aperture jitter stands for the random sampling time variations in ADCs which are caused by broadband noise in the sample and hold circuit. Here it is found that the aperture jitter affects the sampled signal.
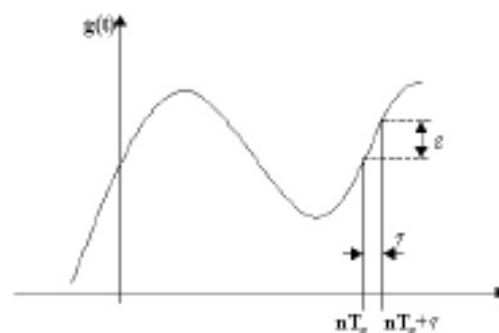

Figure 3: Amplitude error due to aperture jitter

Consider a signal g(t) that is to be sampled, as shown in Figure (3). This signal would ideally be sampled at points that are multiples of Ts, the sampling period. However, due to jitter, sampling does not occur at exactly multiples of Ts, and hence the sampling period varies between samples. This in turn results in an amplitude error. Therefore the uncertainty in sampling position results in an amplitude error of the sampled signal.

The effects of aperture on $\sum\Delta$ ADC can be predicted by the following simple analysis. Assume an input signal is sine wave and is given by the equation

$$v(t) = V_0 sin2\pi f_c t$$

The rate of change of this signal is given by

$$\frac{dv}{dt} = 2\pi f_c V_0 cos2\pi f t \qquad (12)$$

Now let ΔV_{rms} = the rms voltage error and Δt = the rms value of aperture jitter t_j and substitute these values in equation (15).

$$\Delta v_{rms} = \frac{2\pi f_c V_O t_j}{\sqrt{2}} \qquad (13)$$

The rms value of the full-scale input sine wave is $V_o/\sqrt{2}$, the noise produced by aperture jitter is usually modeled as white noise, therefore the signal to noise ratio (expressed in dB) is given by

$$SNR = 20\,log_{10}\left[\frac{V_o/\sqrt{2}}{\Delta v_{rms}}\right] + 10\log(OSR) = 20log_{10}\left[\frac{\frac{V_0}{\sqrt{2}}}{\frac{2\pi f_c V_0 t_j}{\sqrt{2}}}\right] + 10\log(OSR)$$

$$= 20log_{10}\left[\frac{1}{2\pi f_c t_j}\right] + 10\log(OSR)$$

$$(14)$$

Where t_j is the aperture jitter. This amplitude error and hence the signal-to-noise ratio due to jitter becomes worse, if the signal to be sampled varies fast i.e. such as a high frequency carrier. If the deviation of sampling points from the ideal position is large, as deduced from equations above, SNR is poor. Conclusion is that the uncertainty is proportional to the frequency of the input analog signal and it is independent of sampling rate. The equation (14) assumes an infinite resolution ADC where aperture jitter is the only factor determining SNR. It can be proved that the SNR of an ADC is also affected by aperture jitter.

E. *Clock Jitter Effect on Sigma Delta ADC*
Clock jitter is defined as the uncertainty of the sampled signal in time domain due to the uncertainty of the sampling clock [13][17]. It is mainly caused by the instability of the oscillator resulting in sampling time errors in the ADC, therefore degrading the converter's achievable SNR and resolution.
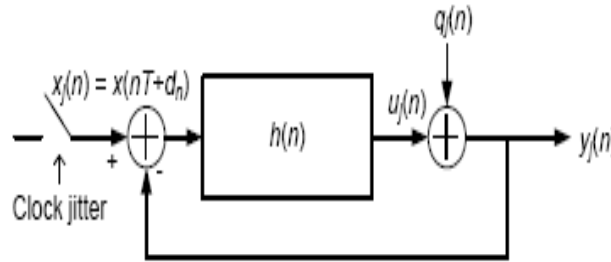

Figure 4: Discrete time $\sum\Delta$ modulator in the presence of clock jitter

Examination of sigma delta modulator in the condition of clock jitter, the output yj(n) now contains error from both the quantization noise and clock jitter, given by:

$$Yj(n) = (x\,(nT + dn) - yj(n))* h(n) + qj(n) \qquad (15)$$

Additional error due to jitter

$$E_y(z) = \left[\frac{1}{1+H(z)}\right]E_q(z) + \left[\frac{H(z)}{1+H(z)}\right]X(z) \qquad (16)$$

IV.   SNR Calculation
In analytical calculations, the clock jitter error and the quantization noise are assumed to be independent of each other. The achievable SNR in the clock jitter condition can be numerically approached (in dB) by

$$SNR = 10log_{10}\left(\frac{P_{signal}}{P_{jitter}+P_{quant}}\right) \qquad (17)$$

Where P_{signal} represent the power of input signal, P_{jitter} and P_{quant} indicate the jitter- triggered error and quantization noise power respectively.

The average noise power due to the clock jitter can then be formulated as follows [17]:

$$P_{signal} = A*A/2 \tag{18}$$
$$P_{quant} = (A*A)/(12*L) \tag{19}$$

Consider a real Analog input signal x(t). In the ADC, x(t) is sampled at the time instant $t_n = nT + J_n$ with the nominal sampling period T. J_n are the random sampling time variations due to aperture jitter and clock jitter. For a block of N sampling point ,the mean error power caused by random jitter process can be calculated as

$$P_j = \frac{1}{N} \sum_{n=0}^{N-1} E\{e(nT) * e(nT)\} \tag{20}$$

where $e(nT) = x(nT + J_n) - x(nT)$

The corresponding error powers due to error :

$$P_j = \frac{1}{N} \sum_{n=0}^{N-1} \sum_{i=-\infty}^{\infty} E\{|e_i(nT)|^2\} \tag{21}$$

The above formula is in time domain, By Fourier transform, the resultant formulae of P_j in frequency domain can be obtained and written as:

$$P_j = \frac{1}{N} \sum_{n=0}^{N-1} \int_{-\infty}^{\infty} S_{ss}(f)(1 - E\{e^{j2\pi Jn}\}) df \, X_{avnfh} \tag{22}$$

Here $S_{ss}(f)$ is the power spectral density(PSD) of x(t).

The Jitter dependent SNR (in Decibels) is given by

$$SNR_j = 10 log \frac{P_s}{P_j} \tag{23}$$

Where $P_{s=} \int_{-\infty}^{\infty} S_{ss}(f) df$

Therefore the SNR_j is

$$SNR_j = 10 log_{10} \left[\frac{\int_{-\infty}^{\infty} S_{ss}(f) df}{\frac{2}{N} \sum_{N=0}^{N-1} \int_{-\infty}^{\infty} Sss(f)(1 - E\{e^{j2\pi Jn}\}) df} \right] \tag{24}$$

Where $S_{ss}(f)$ represents the PSD of input signal, Table 1 shows that performance for different standard with different value of OSR as well as it shows jitter tolerance [19]**.**

V. Simulation Results

In order to confirm the above analysis, some simulation results are presented. Calculation of the SNR at the ADC's output for an maximum input frequency f_c and a sampling frequency $f_s = 2f_c$ has been done while varying the bit resolution. Assumed that the error is due to only the quantization and not due to aperture jitter. For high frequencies above the Nyquist rate, equation 3 is valid. An increase in the sampling rate leads to an increase in the SQNR. For a sampling rate equal to the Nyquist rate (k=1), decrease the quantization noise: the term 10log (k) indicates that it is preferable to use sampling rates as greater than the Nyquist rate as possible (over sampling) because the SQNR has been increased with increasing OSR as shown in fig.(5).
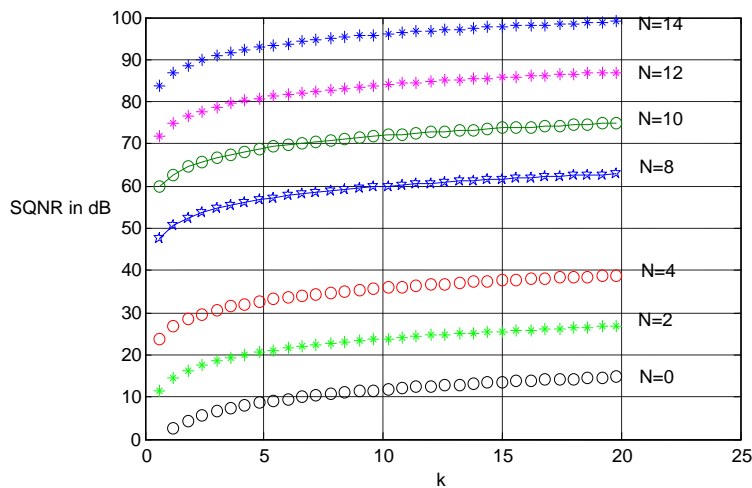

Figure 5: SQNR versus k(oversampling ratio), for N= 2, 8, 10, 12, 14 bits

Figure (6) shows the SNR degradation due to jitter, varying the input frequency (in MHz) with different value of jitter in pico second. In time domain jitter calculation using equation (10), to kept constant number of sample N is 1000 and vary jitter variance 0 to 5*10^-13.,SNR degrades as we increase jitter variance as shown in figure (6). Similarly in figure (7) keep constant jitter variance 0.5*10^-13 and vary the number of samples N, SNR decreases. We improve SNR with jitter by using over sampled   ADC.
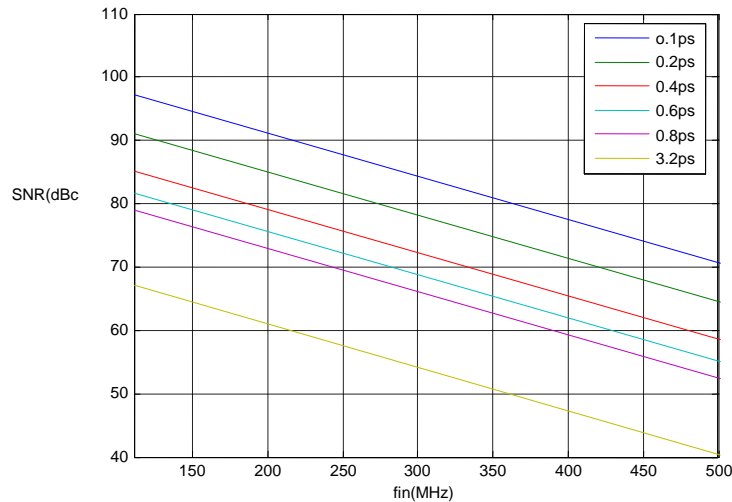
Figure 6: Limitation of SNR due to jitter as a function of input frequency

By using SNR equation (6) of sigma delta ADC, figure (5) shows that as we increase over sampling ratio with order of sigma delta, SNR increases. Table.1 is also given in which effect of SNR and OSR with increase in order of Sigma-Delta ADC and bit resolutions. We calculate effect of clock jitter on Sigma Delta ADC. Greater value of vco leads to the greater SNR reduction. Clock jitter degrades the SNR of the sigma delta ADC.
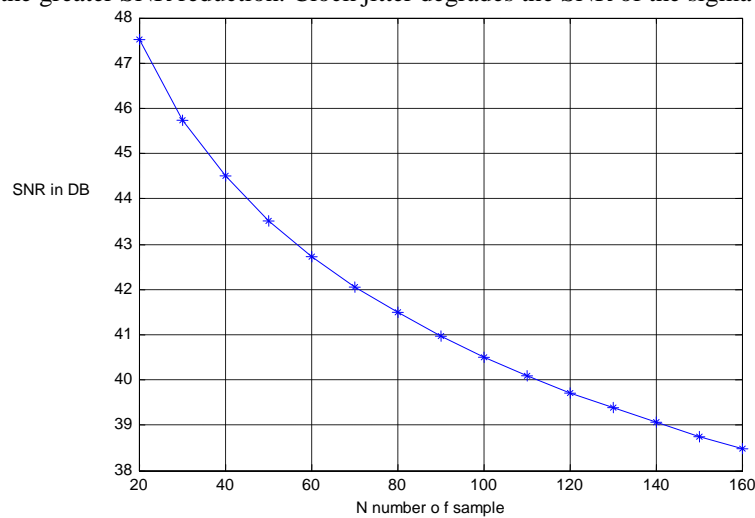

Figure 7: SNR verses N for constant clock jitter variance of 0.5*10^-13

The parameter used as centre frequency fc is 70 MHz sampling frequency f_s is 280 MHz and sampling point N=9*10^6. The values of vco for integrated Oscillator range from 10^19 s to 10^21. In Figure (8), oversampling is expected to improve the system performance by spreading out the quantization noise to a much larger bandwidth. However, this improvement can only be perceived for the low value of OSR. For high value of OSR, the clock jitter noise becomes more dominant compared to the quantization error and leads to the inevitable noise floor.

Table 2: Effect of SNR and OSR with increase in bit resolution of Sigma-Delta ADC (Theoretical Values)

Oversampling factor k	SNR Improvement in dB	Bit resolution
2	3	0.5
4	6	1
8	9	1.5
16	12	2
32	16	2.5
64	18	3
128	21	3.5
256	24	4

Using equation(14),Taking input frequency fc=100MHz aperture jitter is equal to 2ps and sampling rate fs vary from 200MHz to 300MHz Figure(8) shows that as the sampling frequency increases, SNRaj is constant. We conclude that aperture jitter SNR (SNRaj) is independent of sampling rate.
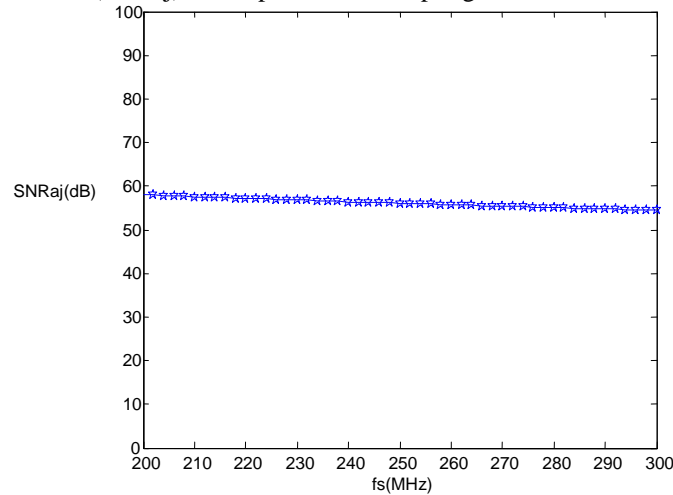

Figure 8: SNRaj versus sampling rate (fs)

Figure 9 shows the aperture jitter power spectrum. The signal was sampled with a sampling frequency of 400 MHz and white Gaussian aperture jitter with a standard deviation (rms aperture jitter) taj = 0.25 ps for fi <<taj^-1 The error power spectrum is white and distributed over whole digitized band. Therefore we increase aperture jitter SNR (SNR_{aj}) by using over sampling technique. But in case of clock jitter, over sampling does not improve the clock jitter SNR (SNR_{clk}). Figure 10 shows the clock jitter's power spectrum which has narrow peaks at ±20MHz and ±90MHz surrounded by Lorentzian shaped spectra which are spread across the spectrum of input signal. The chosen phase noise constant fi<< (vconT) ^0.5. In traditional ADCs, jitter with SNR in between 25-5dB whereas the Sigma Delta ADC has SNR in between 48-38.5db in case of clock jitter and 120-60dBin case of aperture jitter. Jitter tolerance is much better in sigma Delta ADC which is -1*10ps.Sampling technique for improving SNR in case of jitter does not apply on traditional ADC because these ADCs use sample and hold circuit which is an active device and bandwidth of active device is limited. It does not employ on RF or intermediate frequency.
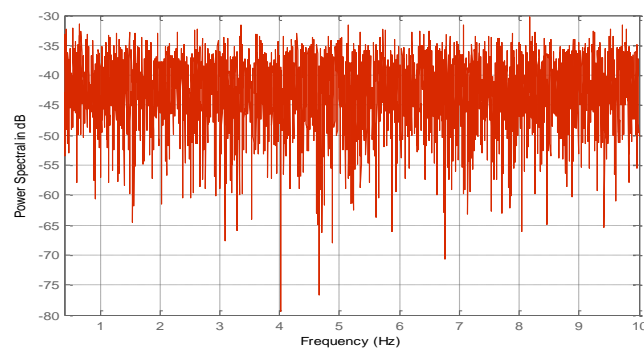

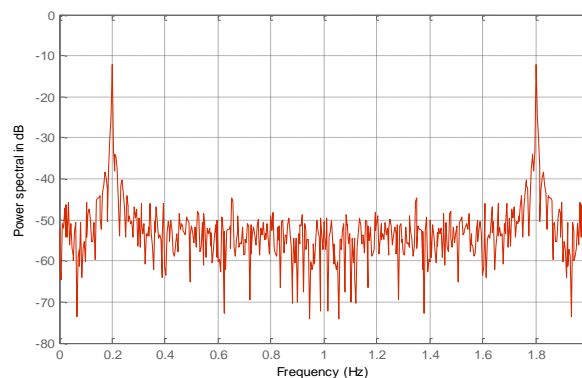**Figure 9: Mean error PSD caused by aperture jitter**

Figure 10: Mean error PSD caused by clock jitter

Simulation of second order sigma delta ADC has been done using MATLAB Simulink. Simulation diagram of second order sigma delta ADC is shown in figure 12. The simulated result for SNR and SQNR is shown in fig. (13). It shows that SNR is 94.8 dB with 256 OSR.

Table 4   Calculated values of SNR and SNDR with respect to OSR

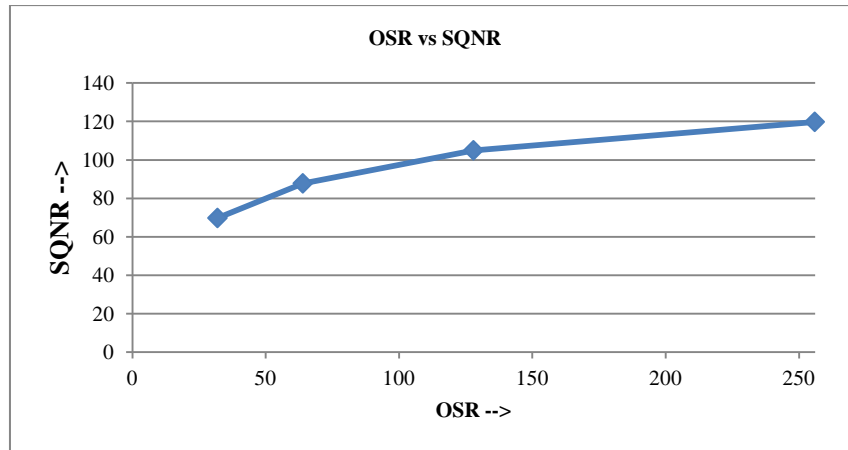| OSR	SNR in dB	SQNR in dB	RESOLUTION(ENOB) (bits)
32	54.8	69.8	8.8
64	69.8	87.8	11.3
128	83.9	105	13.6
256	95.7	119.8	15.6

Figure 11: Theoretical graph of SQNR Vs. OSR
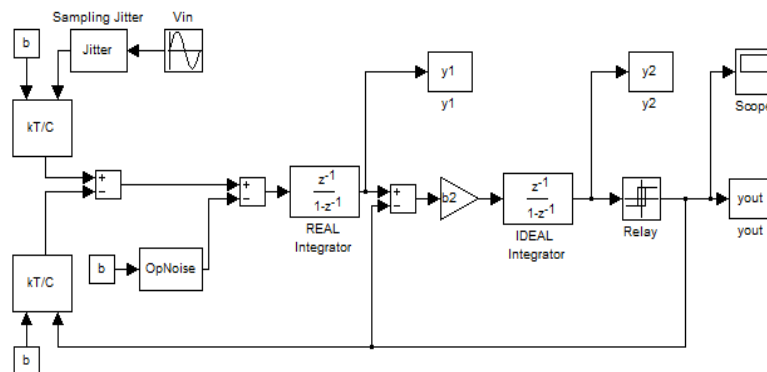

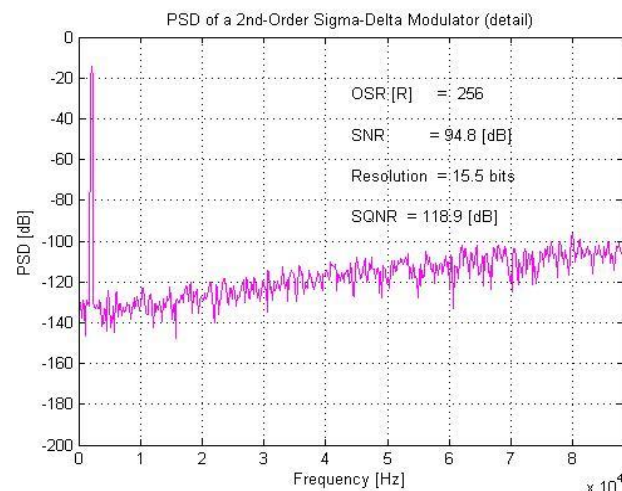**Figure 12: Simulated diagram of second order Sigma Delta ADC**

Figure 13: Simulated result for SNR and SQNR Vs frequency

VI.   Conclusion

This presents that how degradation is there in the system performance due to clock jitter and aperture jitter and concluded that aperture jitter process is stationary as shown in fig (8). Its characteristic functions do not depend on the absolute sampling time instant *nT*, i.e. they are time-invariant. In the case of clock jitter the characteristic functions strongly depend on the absolute sampling time.. Error power spectra of clock jitter and aperture jitter are significantly different. In the case of aperture jitter the mean error power is uniformly distributed over the whole digitization band, so that the jitter dependent SNR in a given frequency band can be increased by over sampling techniques. In the case of clock jitter the error power is concentrated around the frequencies of the input signal components. Analysis shows that Clock jitter is dominating error and severely degrades the system performance in terms of achievable SNR. The SQNR is 118.9dB. 15.5 bits is the Bits of resolution for the second order sigma delta ADC using simulation. Practically it can be considered as 15 bits. Here it can be seen that simulated results are very close to the theoretical results.

References

[1].   J Paul Burns, "Software Defined Radio for 3G", First Edition, Artech House, Boston ,London, 2002, pp. 51-70.
[2].   J.H. Reed , "Software Radio –A modern approach to radio engineering" Peason   Education , 2002.
[3].   S. Haykin, Communication Systems, John Wiley & Sons Inc, ch. 6, pp. 374-378.
[4].   J.C. Candy and G.C. Temes, Oversampling Delta-Sigma Data Converters. IEEE Press, New York, 1992 .
[5].   R.T.Baird and T.S.Fiez, "Stability Analysis of High-Order Delta-Sigma Modulation for ADC's," IEEE Trans Circuit Syst.II.vol. 41, pp. 59-62, Jan 1999.
[6].   S. S. Awad, "The effects of accumulated timing jitter on some sine wave Measurements," IEEE Trans.Instrum. Meas.,vol. 44, pp. 945–951, Oct. 1995.
[7].   Selim saad Awad "Analysis of Accumulated Timing-jitter in Time Domain," IEEE transaction on Instrumentation and measurement, Vol. 47, No. 1, Feb 1998.
[8].   H. Tao, L. T´oth, and John M. Khoury, "Analysis of Timing Jitter in Band   pass Sigma-Delta Modulators,"IEEE Transactions on Circuits and Systems—Part II: Analog and Digital Signal Processing, vol.46, no. 8, pp. 991–1001, 1999.
[9].   R. Meyer, "Software-Defined-Radio Technology Targets 3G Designs ",Wireless   Systems Design,vol. 5, no. 2, pp. 16-20, 2002.
[10].   Joseph Mitola and Zoran Zvonar,"Software and DSP in radio,"IEEE Communication Magazine, Feb 2000 .
[11].   R. H. Walden, "Analog-to-Digital Converter Survey and Analysis," IEEE Journal on Selected Areas in   Communications, vol. JSAC-17, no. 4, pp. 539– 550, Apr. 1999.
[12].   Alper Demir, Amit   Mehrotra, and Jaijeet Roychowdhury, " Phase Noise in Oscillators:A Unifying Theory and Numerical Methods for Characterization"IEEE transaction on Circuit and System-I; Fundamenta Theory and Application   Vol, 47, No.5, May2000.
[13].   H. Kobayashi, M.Morimura, K. Kobayashi, and Y. Onaya, "Aperture Jitter Effects in Wideband ADC Systems," in Proc. of the 6th IEEE International Conference on Electronics, Circuits and Systems (ICECS '99), Pafos, Cyprus, Sept. 1999, pp. 1705-1708.
[14].   A Hairong Chang, Hua Tang, " Simple Technique to Reduce Clock Jitter Effects in   Continuous-Time Delta- Sigma Modulators", IEEE International symposium on Circuits and Systems (ISCAS) 2007.
[15].   Neil Roberts, "Understanding phase noise and jitter," High-performance Analog Designer Zarlink Semiconductor Inc.
[16].   Planet Analog, "Understanding Analog/digital Converter clock jitter-and why you should care"2007.
[17].   Eduardo Bartolome**,** Vineet Mishra, Goutam Dutta and David Smith, "clocking high-speed data converters", Texas Instruments Incorporated 2008.
[18].   U Derek Redmayne, Eric Trelewicz and Alison Smith, "understanding the effect of clock jitter on high-speed ADCs Linear Technology" published by Linear Technology.
[19].   M.Lohning and G. Fettweis, "The effects of aperture jitter and clock jitter in Wideband ADCs," International Journal Computer Standard and Interfaces (CS&I), vol. 29(1), pp. 11–18, January 2007.
[20].   Bakti Darma Putra and Gerhard Fettweis, "Effect of Clock Jitter on the Performance of Band pass sigma delta ADCs," ISCCSP-08 proceedings, pp. 67-74, 2008.