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Comparative Analysis of Positive Feedback and Darlington Pair based Operational Amplifier at 32m Technology

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***Abstract**: Operational amplifiers are employed in several applications including: low-dropout voltage regulators, audio amplifiers and filters. Most of the applications require Op-Amp with improved gain, minimum leakage current, low power along with the high bandwidth. But it is essential to provide a wide range of bandwidth without influencing other performance metrics drastically. In this paper, the positive feedback technique has been described and a novel Darlington Pair approach has been taken to implement an ultra low power high gain CMOS two stage Operational Amplifier. This approach ameliorates gain bandwidth product (GBW) and also confers high gain in 32nm technology. The circuit is simulated at 1V power supply at Room temperature.*

I. Introduction

Op-Amp emerged as a main design block in the analog circuit applications and dominated the market. The situation is now-a-days changing. The modern linear ICs Op-Amp works at lower voltage [1]. Because of their reduced size, versatile and flexible nature, Op-Amps are use in the fields of process control, communications, computers, power and signal source, displays and measuring systems. It is basically termed as a high gain direct coupled amplifier. Analog as well as digital circuits and systems employ Op-Amps as a basic building block. Op-Amp performs arithmetic operations such as addition, subtraction, division, multiplication, integration, differentiation etc.

The "Gorden Moore" envisioned that, the number of transistors per chip would quadruple every three years. The shrinking of CMOS technology has been increased every aggressively with ultra-thin sizes [2]. Operational Amplifiers (Op-Amps) are such a crucial component among various analog systems. Operational amplifiers are considered as a crucial building block in analog and mixed circuit systems and the main goal for designing is to ameliorate performance and use the small size components. An operational amplifier can also be defined as a direct coupled high gain amplifier. Basically, the number of amplifier stages appended in a complex way, thus why it is a multistage amplifier [3]. Its internal circuitry comprises of many transistors, resistors and occupies less space. Thus it employs a little package and is exist in the Integrated circuit (IC) form.

II. Conventional Two-Stage CMOS Op-Amp

Two-stage Op-Amp are the most popular among general purpose Op-Amp because much larger gain can be obtained compared to single stage Op-Amp. Two-stage refers to the number of gain stage in the Op-Amp [4]. The basic two-stage Op-Amp comprises of Two-Stage: first is differential amplifier stage and other is common source stage. Since Op-Amps generally do not employ output buffer so it is limited to drive resistive loads and high capacitive loads [5].

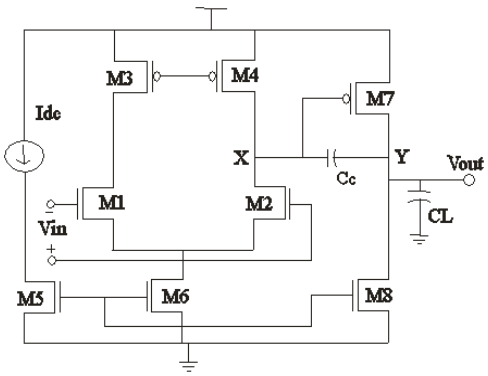

Figure 1: Schematic diagram of Two-Stage Op-Amp

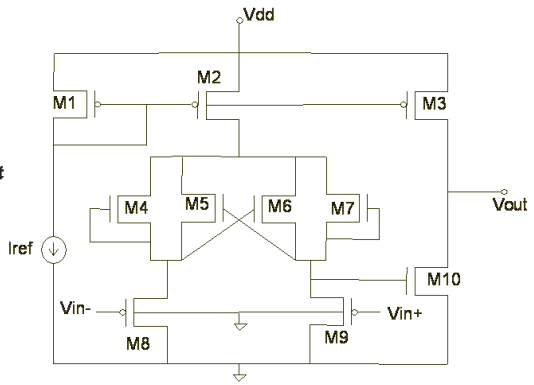

Figure 2: Schematic diagram of CMOS two-stage Op-Amp with positive feedback at load.

III. Positive Feedback

Applying positive feedback at load of differential pair of Op-Amp increases the overall DC gain, CMRR and reduced the power consumption and leakage current. One dominant dilemma allied along the function of positive feedback within Op-Amp is the chances of uncontrollability. Though, an Op-Amp employing positive feedback perhaps balanced if it is created accurately during the speculating that the overall gain of the amplifier is meager. One more obstacle affiliated with usage of positive feedback is the tenacious dependency of overall DC gain of the Op-Amp [6]. To overcome this problem transistor matching should be accurately. And all of these complications are handled by choosing W/L ratio exactly.

Figure 2 shows the illustrative diagram of CMOS two stage Op-Amp with positive feedback at load of the differential amplifier [7]. The Operational Amplifier designed here is un-buffered. It is also widely known as Operational Trans-conductance Amplifier (OTA). Since the operational amplifier is un-buffered, the output impedance of the circuit will be high [8].

DC gain equation of figure 2 can be written as

$$A_d = \frac{-g_{m8}}{(g_{ds8} + g_{ds4} + g_{ds5} + g_{m4} - g_{m5})} \quad (1)$$

Where g_{ds8}, g_{ds4}, g_{ds5} are the output conductance and g_{m8}, g_{m4} and g_{m5} are the conductance of M8, M4, M5 respectively.

IV. Darlington Pair

In recent times the increasing the requirement of Darlington devices for the high data rate communication system [9] .Where a high signal is required at particular low frequency along with high selectivity for present-day professional application high gain and high bandwidth is require Darlington topology and Darlington cell [10].

The Darlington pair based two stage CMOS operational amplifier is shown in figure 3. In this, use of biasing current source I_{BIAS} is to establish the quiescent DC operating current in the Darlington pair transistor D1. Effective values of the g_m and r_o of the composite device M10 and M11 will be calculated.

$$GB = \frac{g_{m7}}{C_{gs6,7}} \quad (2)$$

Where GB= Gain Bandwidth, G_m= Trans-conductance, C_{gs}= Gate to Source capacitance

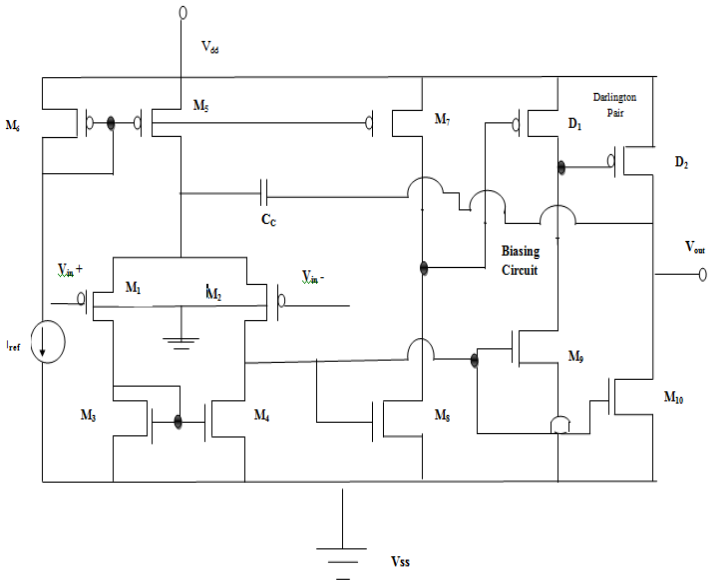

Figure 3: CMOS Two-Stage Op-Amp with Darlington Pair

However, a dominant shortcoming confronted along with its performance. At peak frequencies its feedback turns into weaker than that of a single transistor amplifier. To overthrown this dilemma, so many modifications are applied in Darlington pair amplifiers either by including some additional biasing resistances in the device or by applying Triple Darlington topology the previous published Darlington amplifiers [11].

V. Simulation & Results

The presented circuit is simulated at 32nm technology with the help of spice tool. Channel length of each transistor is 32nm. The Op-Amp operates at low supply voltage of 1V at room temperature. Simulation results of both the technologies are compared in table 1.

Table 1: Comparative analysis of Positive Feedback and Darlington Pair Technique.

Performance Parameter	Positive Feedback	Darlington Pair
Supply Voltage (Volt)	1	1
Technology (nm)	32	32
Gain (dB)	87	93
CMRR (dB)	86	100
Slew Rate (V/µS)	20.13	21
Power Dissipation (pW)	66	50
Leakage Current (pA)	4.21	2.17
Phase Margin (degree)	86	86
Unity Gain Bandwidth (MHz)	223	538
Settling Time (nS)	95	95

Figure 4 depicts the comparison of leakage current measured in two-stage Op-Amp through Positive Feedback and Darlington Pair. There is about 2þA decrement in Darlington Pair.

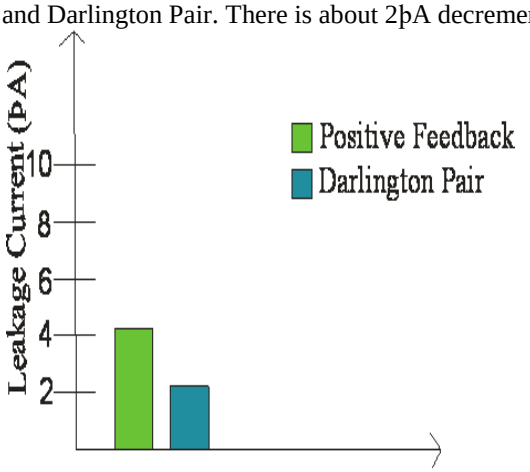

Figure 4: Comparison of leakage current.

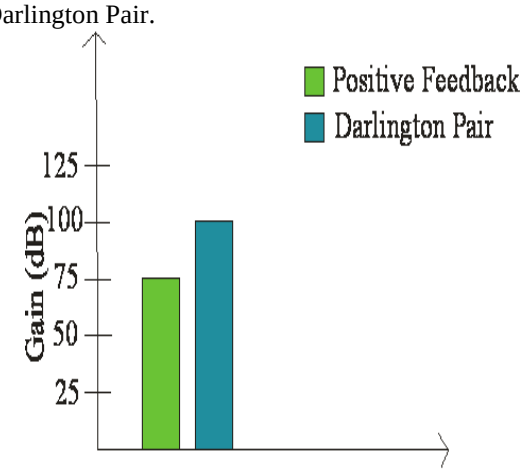

Figure 5: Comparison of gain

Figure 5 illustrates the gain obtained through Positive Feedback and Darlington Pair. It is noticed from figure that gain is increased about 6 dB in Darlington Pair.

Figure 6 demonstrates the comparison of CMRR that obtained from Positive Feedback and Darlington Pair. 100 dB CMRR is achieved from Darlington Pair.

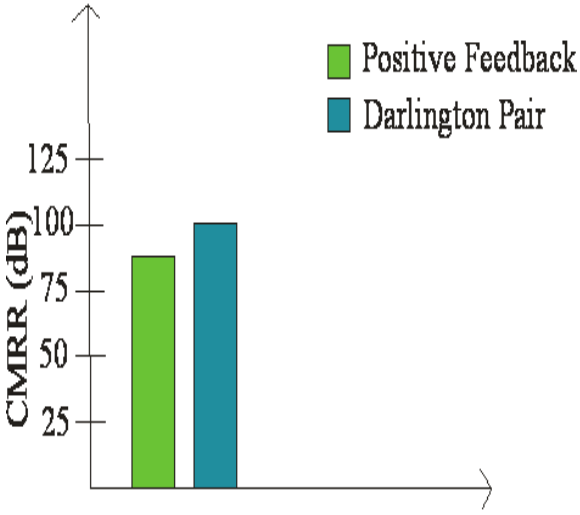

Figure 6: Comparison of CMRR

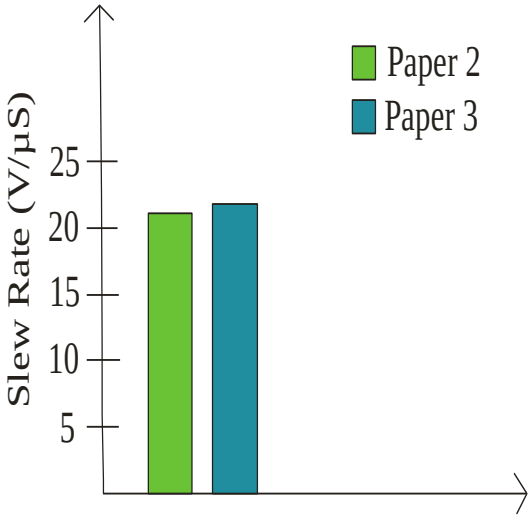

Figure 7: Comparison of Slew Rate

Figure 7 depicts the comparison of Slew Rate which obtained through Positive Feedback and Darlington Pair. 20.13 V/µS and 21V/µS slew rate is achieved through positive feedback and Darlington pair respectively.

From these figures it is clear that Darlington Pair two-stage Op-Amp has better performance parameter as compared to Positive Feedback two-stage Op-Amp.

VI. Conclusion

The design of a compact low-power low-voltage two stage CMOS Op-Amp has been discussed and simulated at 32nm Technology. In this paper, a modern access has been granted for designing immense gain amplifiers. The differential stage of the CMOS two stage Op-Amp has been customized and Positive Feedback strategy and Darlington Pair were successfully materialized for obtaining this extensively giant gain. Despite of it, there is a need of high level transistor matching for implementing positive feedback technique, which causes the designing procedure complicated.

VII. References

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