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FFT based DTMF detection by using Spartan 3E FPGA

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Abstract*: DTMF is a method of representing the digits with tones for transmission. Dual Tone Multi Frequency (DTMF) tones are used by all touch tone phones to represent the digits on a touch tone keypad. DTMF technology provides a robust alternative to rotary telephone systems and allows user-input during a phone call. This feature has enabled interactive, automated response systems such as the ones used for routing customer support calls, telephone banking, voicemail, and other similar applications. This paper explains about the FFT based DTMF detection by using Spartan 3e FPGA. FFT based Technique is basically used for detecting the DTMF. Mentor Graphics Modelsim Xilinx Edition (MXE) is used for the Functional Verification and Xilinx ISE is used for Synthesis & simulation respectively. The Xilinx Spartan 3e FPGA Family board is used in this paper.*

Keywords*: FFT; DTMF; Xilinx ISE; Modelsim; Spartan 3E FPGA*

I. INTRODUCTION

Dual Tone Multiple Frequency (DTMF) signaling is used in telephone dialing, interactive banking systems, digital answer machines. DTMF signaling represents each symbol on a telephone touchtone keypad (0 to 9, *, #, A-D) using two sinusoidal tones, as shown in Fig. 1. When a key is pressed, a DTMF signal consisting of a row frequency tone plus a column frequency tone is transmitted. Keys A,B,C,D are not on commercial telephone sets, but are used in military and radio signalling applications. The maximum dialling rate is 10 symbols/s in the Bellcore standard [1], [2] and 12.5 symbols/s in the International Telecommunication Union (ITU) Q.24 standard [3].

ITU specifications require that, the valid DTMF signals have their high and low frequency tones within a tolerance of ±1.5% of an ideal DTMF frequency. If the tolerance of either tone is outside ±3.5%. Then the signal should be rejected as invalid. ITU specifications place requirements on the duration, and pauses between valid DTMF signals. ITU specifications require 100% detection of valid DTMF signals at 15 dB SNR (Signal to Noise Ratio). Bellcore provides test tapes to measure the performance of a DTMF detector against talk-off, which is false detection of speech signals as DTMF signals.

Fig.1 DTMF Scheme for Touch Tone Dialing (Courtesy from IEEE Transactions on Signal Processing)

II. PROPOSED ARCHITECTURE DESIGN

The proposed Architecture can be showed in Fig.2.

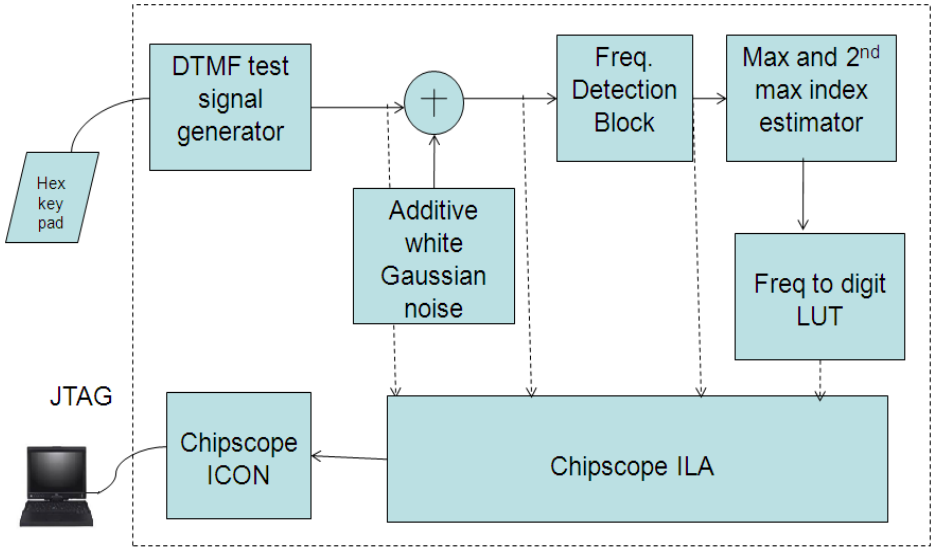

Fig.2 DTMF Detection General Module

It consists of the following modules:

1. Hex key pad
2. DTMF signal generator
3. Additive white Gaussian noise
4. Frequency Detection block
5. Magnitude / index estimator
6. Frequency to digit look-up table

1. Hex keypad:

The Hex Keypad gives the input to the module. It is an external component. The signal from column is taken as input. Row and display are the output signals.

2. DTMF test signal generator:

The DTMF test signal generator block generates that, the carrier frequencies necessary. It consists of two blocks

2.1 Frequency word selector:

In this block the carrier waves are generated according to the key pressed 'o'.

For example:

If key 9 is being press the frequencies that are generated are 852 Hz (Low frequency group) & 1477 Hz (High frequency group). These frequency waves are generated by a DDS core.

2.2 DDS Core:

The LogiCORE™ IP DDS (Direct Digital Synthesizer) Compiler core sources sinusoidal waveforms for use in many applications. A DDS consists of a Phase Generator and a SINE/COS Lookup Table. These parts available individually or combined via this core. Direct digital synthesis (DDS) is a method of producing an analog waveform—usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. With advances in design and process technology, today's DDS devices are very compact and draw little power.

3. Additive white Gaussian Noise:

The tone out, which is the output from tones generator is mixed with noise in this module. The output is named as noise bits. Wideband Gaussian noise comes from the many natural sources, such as the thermal vibrations of atoms in conductors (referred to as thermal noise or Johnson-Nyquist noise), shot noise, black body radiation from the earth and other warm objects, and from celestial sources such as the Sun. The AWGN channel is a good model for many satellite and deep space communication links. It is not a good model for most terrestrial

links because of multipath, terrain blocking, interference, etc. However, for terrestrial path modeling, AWGN is commonly used to simulate background noise of the channel under study, in addition to the multipath, terrain blocking, interference, ground clutter and self interference that modern radio systems encounter in terrestrial operation.

4. Tone Generator:

The main propose of Tone Generator block is take two cosine waves from DDS cores and add them in order to produce one wave called tone out.

5. Frequency Detector:

Input to the Frequency Detector module is noise bits, which is the output from additive white Gaussian noise.

6. The Output of the block is indices and magnitudes. As per the scope of the project, there are three variants of frequency detector block

1. FFT-128 core
2. Goertzel algorithm
3. Resource sharing

This paper presents about FFT based DTMF Detection.

III. FFT - 128 CORE

FFT- 128 core: The below figure represents the FFT core as a Frequency detector module.

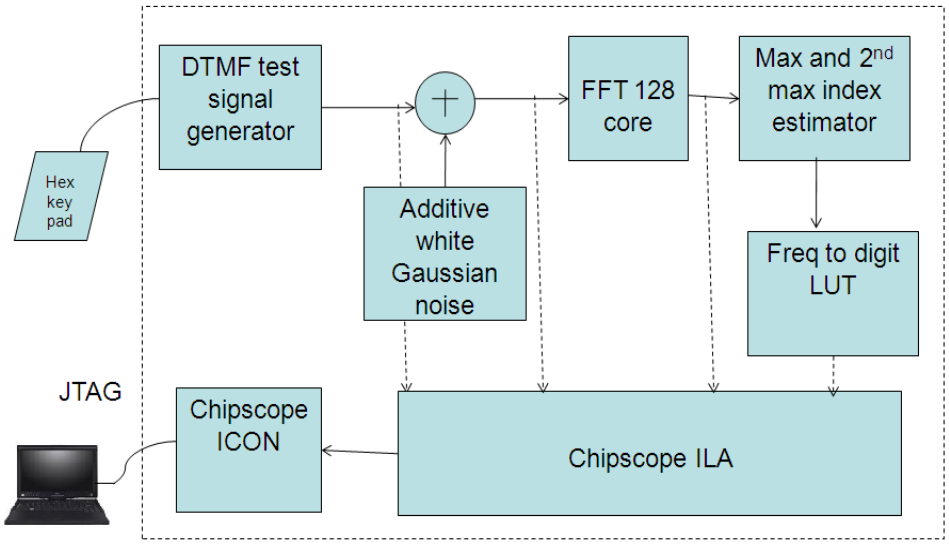

Fig.3 Block Diagram with FFT-128 Core as Frequency Detection Module

The Xilinx LogiCORE™ IP Fast Fourier Transform (FFT) implements the Cooley-Tukey FFT algorithm, a computationally efficient method is for calculating the Discrete Fourier Transform (DFT). A fast Fourier transform (FFT) is an efficient algorithm to compute the discrete Fourier transform (DFT) and it's inverse. There are many distinct FFT algorithms involving a wide range of mathematics, from simple complex-number arithmetic to group theory and number theory.

A DFT decomposes a sequence of values into components of different frequencies. This operation is useful in many fields (see discrete Fourier transform for properties and applications of the transform) but computing it is directly from the definition is often too slow to be practical. An FFT is a way to compute the same result more quickly: computing a DFT of N points in the naive way, using the definition, takes $O(N^2)$ arithmetical operations, while an FFT can compute the same result in only $O(N \log N)$ operations.

The difference in speed can be substantial, especially for long data sets where N may be in the thousands or millions in practice, the computation time can be reduced by several orders of magnitude in such cases, and the improvement is roughly proportional to $N/\log(N)$. This huge improvement made many DFT-based algorithms practical; FFTs are of great importance to a wide variety of applications, from digital signal processing and solving partial differential equations to algorithms for quick multiplication of large integers.

The most well known FFT algorithms depend upon the factorization of N, but (contrary to popular misconception) there are FFTs with O (N log N) complexity for all N, even for prime N. Many FFT algorithms only depend on the fact that $e^{-\frac{2\pi i}{N}}$ is an N th primitive root of unity, and thus can be applied to analogous transforms over any finite field, such as number-theoretic transforms.

IV. SIMULATION RESULTS

The below figures can represents the simulation results of FFT based DTMF Detection with maximized view by using MODELSIM.

FFT based DTMF Detection:

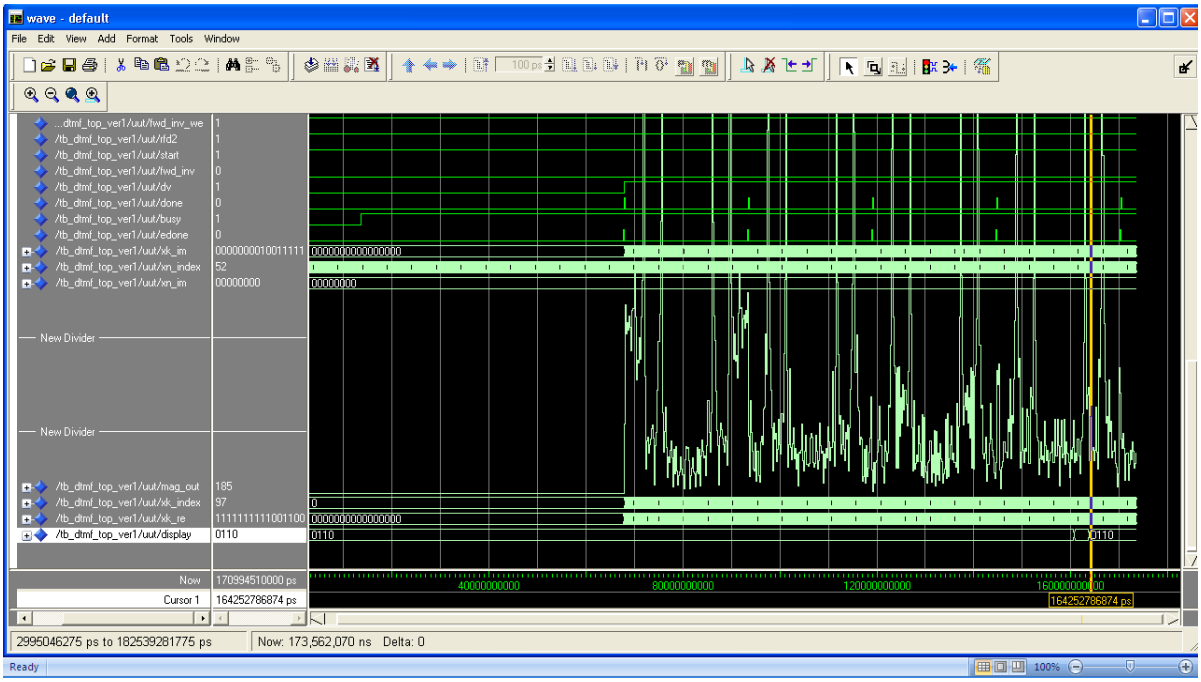

Fig. 4 Simulation Results of FFT

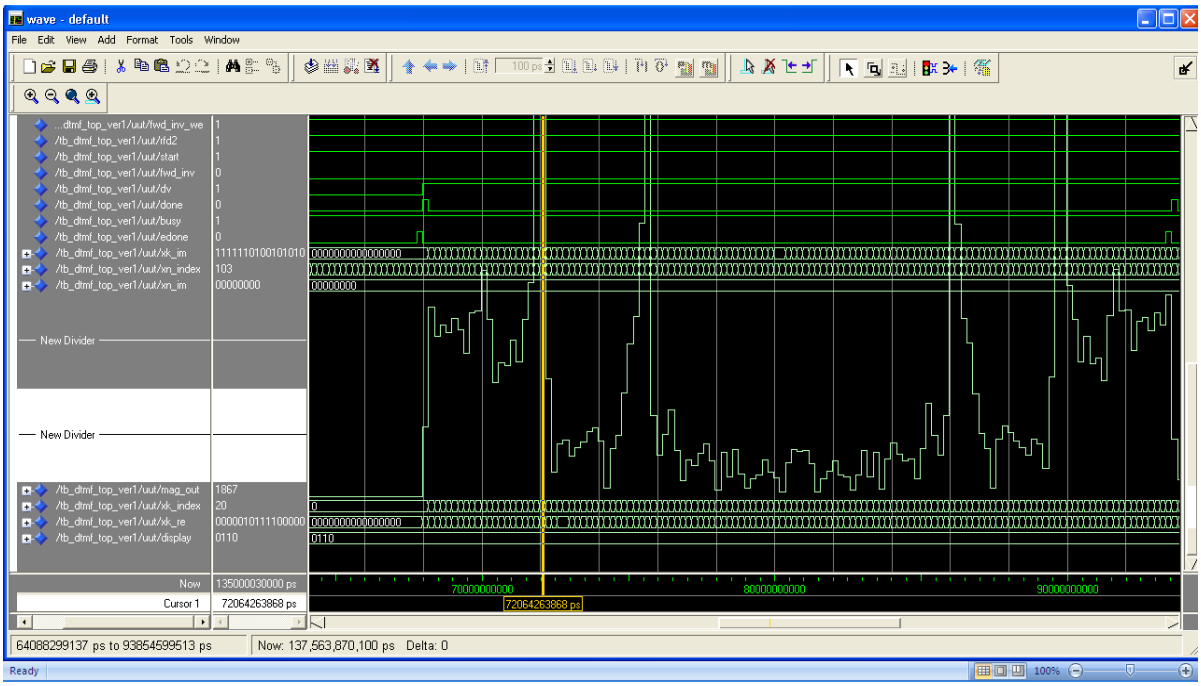

Fig. 5 Simulation Results of FFT in Maximized View

V. SYNTHESIS REPORT

Synthesis Report for FFT based DTMF Detection:

Device utilization summary:

Selected Device: 3s500efg320-4

Number of Slices	: 2646 out of 4656 56%
Number of Slice Flip Flops	: 3256 out of 9312 34%
Number of 4 input LUTs	: 4268 out of 9312 45%
Number used as logic	: 2589
Number used as Shift registers	: 431
Number used as RAMs	: 1248
Number of IOs	: 35
Number of bonded IOBs	: 31 out of 232 13%
Number of GCLKs	: 2 out of 24 8%

Timing Summary:

Speed Grade: -5

Minimum period	: 17.669ns (Maximum Frequency: 56.596MHz)
Minimum input arrival time before clock	: 7.265ns
Maximum output required time after clock	: 18.417ns
Maximum combinational path delay	: No path found

VI. CONCLUSION

This paper presents about the FFT based DTMF detection by using Spartan 3e FPGA because of FPGA technology is increasing its applications in communication technologies. The area, timing and power results are analyzed. For this design the Speed Grade Minimum period is 17.669ns (Maximum Frequency: 56.596MHz), Minimum input arrival time before clock is 7.265ns, Maximum output required time after clock is18.417ns. In future this paper will extend to Goertzel Algorithm based DTMF detection by Using Resource Sharing Approach on High Speed FPGSs like Virtex SP6 & Zynq 7000 series FPGA family.

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